

TC518128CPL/CSPL/CFL/CFWL/CFTL-70/80/10 TC518128CPL/CSPL/CFL/CFWL/CFTL-70L/80L/10L

SILICON GATE CMOS

PRELIMINARY

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128C is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128C utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128C operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128C features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128C is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic package, and a 32-pin thin small outline plastic package (forward type).

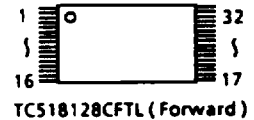
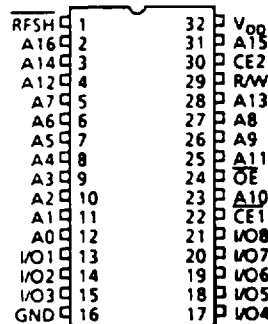
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518128C Family		
	-70	-80	-10
t_{CEA} CE Access Time	70ns	80ns	100ns
t_{OEA} OE Access Time	25ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	100µA (L version) 50µA (LL version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
 - TC518128CPL : DIP32-P-600
 - TC518128CFL : SOP32-P-450
 - TC518128CSPL : DIP32-P-300
 - TC518128CFWL : SOP32-P-525
 - TC518128CFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518128CPL/CFL/CSPL/CFWL

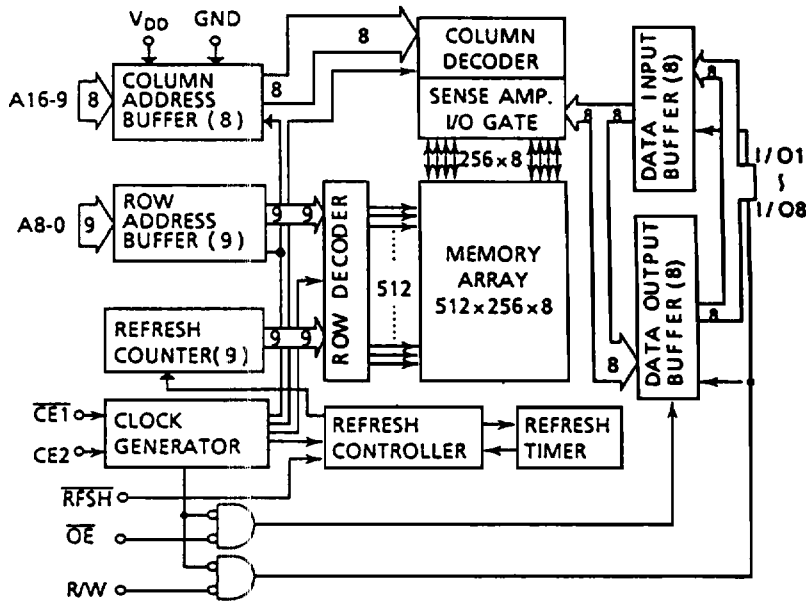
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
RFSH	Refresh Input
CE1, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A ₁₀	OE

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	\overline{RFSH}	A0 - A16	I/O1 - 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
CE only Refresh		L	H	H	H	*	V*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Auto/Self Refresh		*	L	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ
Standby		*	L	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of $\overline{CE1}$ ($CE2 = H$) or the rising edge of CE2 ($\overline{CE1} = L$), all address inputs are latched. At all other times, the address inputs are **.

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	–	V _{DD} + 1.0	V	
V _{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES	
I _{DDO}	Operating Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	–	50	70	mA 3,4	
		80ns version	–	40	60		
		100ns version	–	35	50		
I _{DDs1}	Standby Current CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IH}	–	–	1	mA		
I _{DDs2}	Standby Current CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = V _{DD} - 0.2V	L version	–	50	100	μA	
		LL version	–	35	50	μA	
I _{DDF1}	Self Refresh Current (Average) CE1 = V _{IH} or CE2 = V _{IL} , RFSH = V _{IL}	–	–	1	mA		
I _{DDF2}	Self Refresh Current (Average) CE1 = V _{DD} - 0.2V or CE2 = 0.2V, RFSH = 0.2V	L version	–	50	100	μA	
		LL version	–	35	50	μA	
I _{DDF3}	Auto Refresh Current (Average) RFSH cycling: t _{RC} = t _{RC} min	–	–	2	mA		
I _{DDF4}	CE only Refresh Current (Average) CE1, CE2, Address cycling: t _{RC} = t _{RC} min.	70ns version	–	50	70	mA 3	
		80ns version	–	40	60		
		100ns version	–	35	50		
I _{IL} (L)	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	–	–	±10	μA		
I _{OL} (L)	Output Leakage Current Output Disabled (CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or R/W = V _{IL}), 0V ≤ V _{OUT} ≤ V _{DD}	–	–	±10	μA		
V _{OH}	Output High Level I _{OH} = -1mA	2.4	–	–	V		
V _{OL}	Output Low Level I _{OL} = 2.1mA	–	–	0.4	V		

Note: For I_{DDs1} and I_{DDF1} with CE1 = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL} (CE1 = V_{IH} or CE1 = V_{IL}).
For I_{DDs2} and I_{DDF2} with CE1 ≥ V_{DD} - 0.2V (CE2 ≤ 0.2V), the specified limits are guaranteed under the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V (CE1 ≥ V_{DD} - 0.2V or CE1 ≤ 0.2V).

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C _{I2}	Input Capacitance (CE1, CE2, OE, R/W, RFSH)	–	7	
C _{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

TC518128CPL/CSPL/CFL/CFWL/CFTL-70/80/10
 TC518128CPL/CSPL/CFL/CFWL/CFTL-70L/80L/10L Static RAM

AC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%) (Notes: 5, 6, 7, 8)

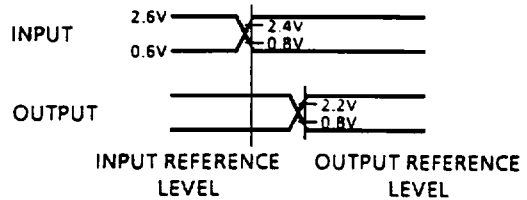
SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	–	130	–	160	–	ns	
t _{RMW}	Read Modify Write Cycle Time	160	–	180	–	220	–		
t _{CE}	CE Pulse Width	70	10,000	80	10,000	100	10,000		13
t _p	CE Precharge Time	35	–	40	–	50	–		
t _{CEA}	CE Access Time	–	70	–	80	–	100		
t _{OEA}	OE Access Time	–	25	–	30	–	40		
t _{CLZ}	CE to Output in Low -Z	20	–	20	–	20	–		
t _{OLZ}	OE to Output in Low -Z	0	–	0	–	0	–		
t _{WLZ}	Output Active from End of Write	0	–	0	–	0	–		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	OE Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{ODS}	OE Output Disable Setup Time	0	–	0	–	0	–		
t _{ODH}	OE Output Disable Hold Time	10	–	10	–	10	–		
t _{RCS}	Read Command Setup Time	0	–	0	–	0	–		
t _{RCH}	Read Command Hold Time	0	–	0	–	0	–		
t _{WP}	Write Pulse Width	20	–	25	–	30	–		
t _{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t _{CWL}	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000		
t _{DSW}	Data Setup Time from R/W	15	–	20	–	25	–		10
t _{DSC}	Data Setup Time from CE	15	–	20	–	25	–		10
t _{DHW}	Data Hold Time from R/W	0	–	0	–	0	–		10
t _{DHC}	Data Hold Time from CE	0	–	0	–	0	–		10
t _{ASC}	Address Setup Time	0	–	0	–	0	–		11
t _{AHC}	Address Hold Time	20	–	25	–	30	–		11
t _{RHC}	RFSH Command Hold Time	15	–	15	–	15	–		
t _{FC}	Auto Refresh Cycle Time	115	–	130	–	160	–		
t _{RFD}	RFSH Delay Time from CE	35	–	40	–	50	–		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t _{FP}	RFSH Precharge Time	30	–	30	–	30	–	12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	12	
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	160	–	160	–	190	–	12	
t _{REF}	Refresh Period (512 cycles, A0 – A8)	–	8	–	8	–	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t _{CES}	CE2 Low Setup Time	5	–	5	–	5	–	ns	14
t _{CEH}	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels	:	$V_{IH} = 2.6V$ $V_{IL} = 0.6V$
Input Reference Levels	:	$V_{IH} = 2.4V$ $V_{IL} = 0.8V$
Output Reference Levels	:	$V_{OH} = 2.2V$ $V_{OL} = 0.8V$



8) Measured with a load equivalent to 1 TTL load and 100pF.

9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .

12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.

- Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
- Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

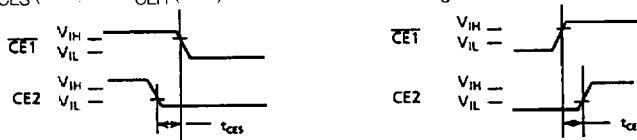
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.

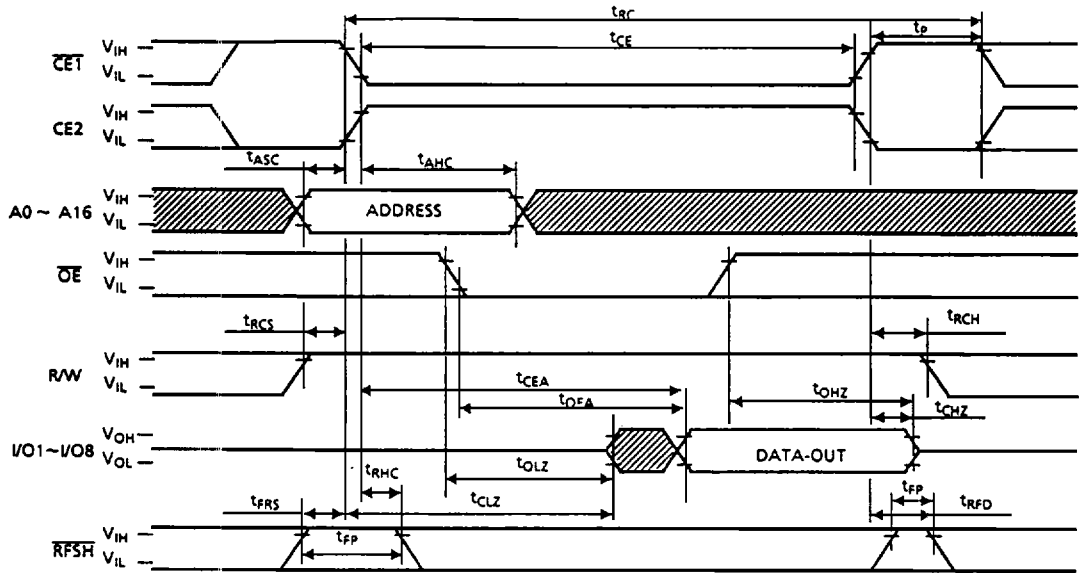


14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.

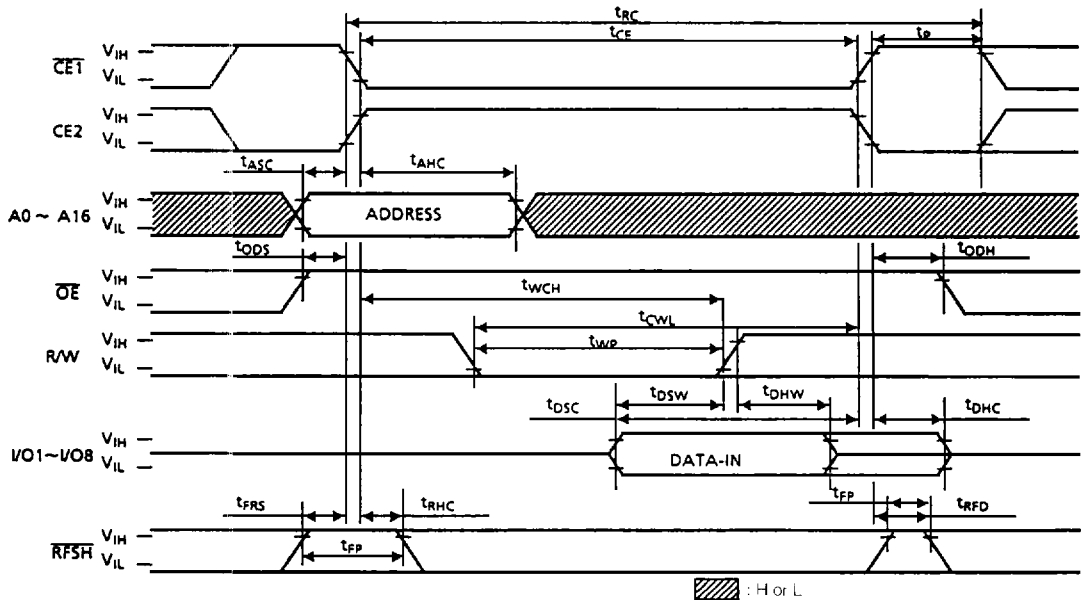


Timing Waveforms

Read Cycle

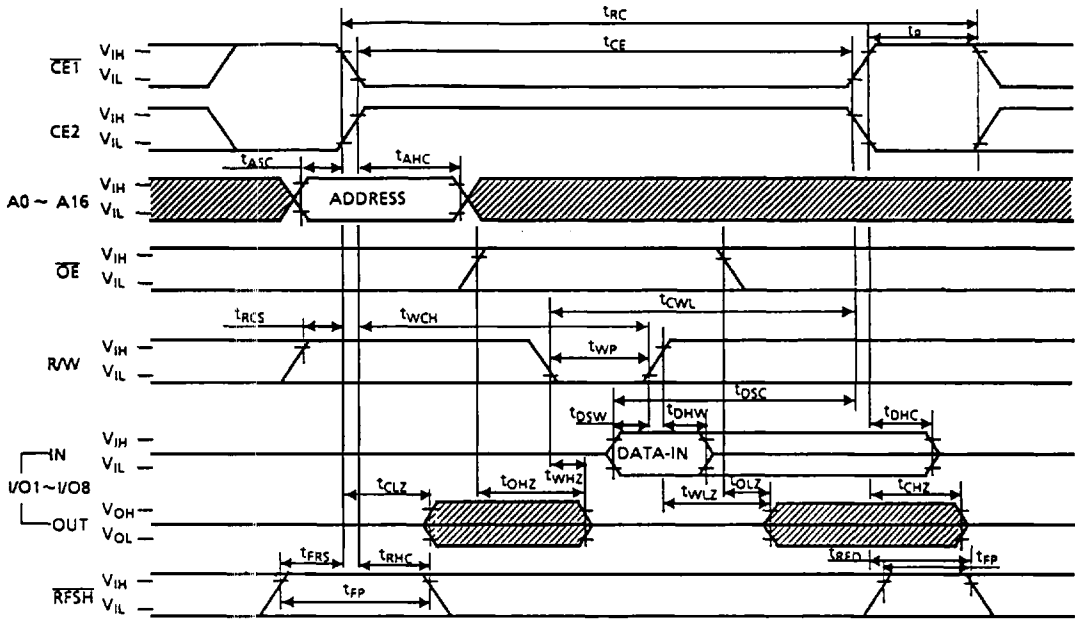


Write Cycle 1 (\overline{OE} Fixed High)

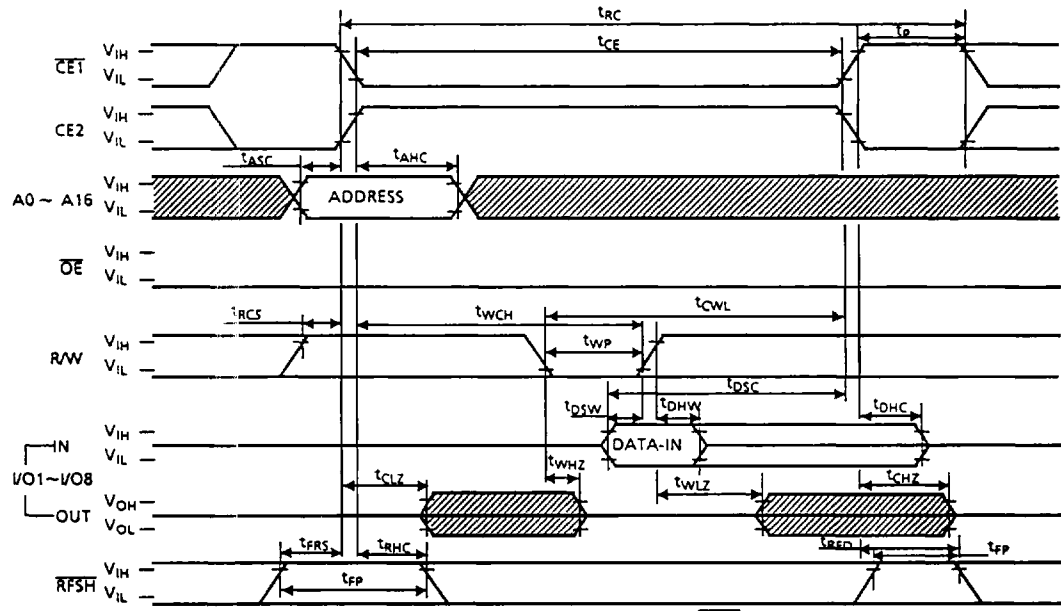


Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 (\overline{OE} Clocked)



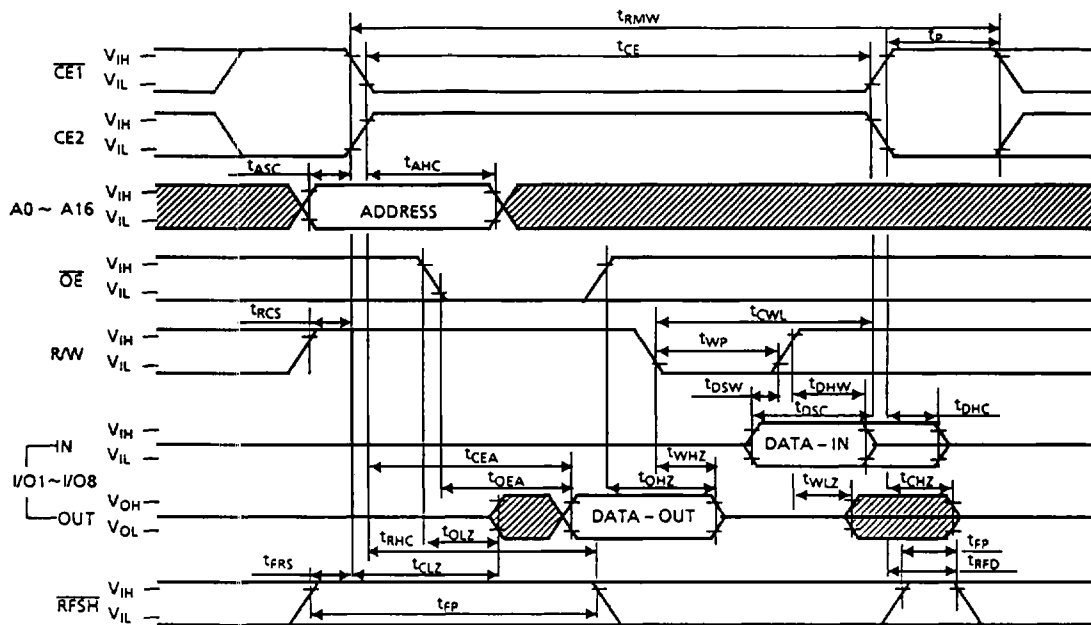
Write Cycle 3 (\overline{OE} Fixed Low)



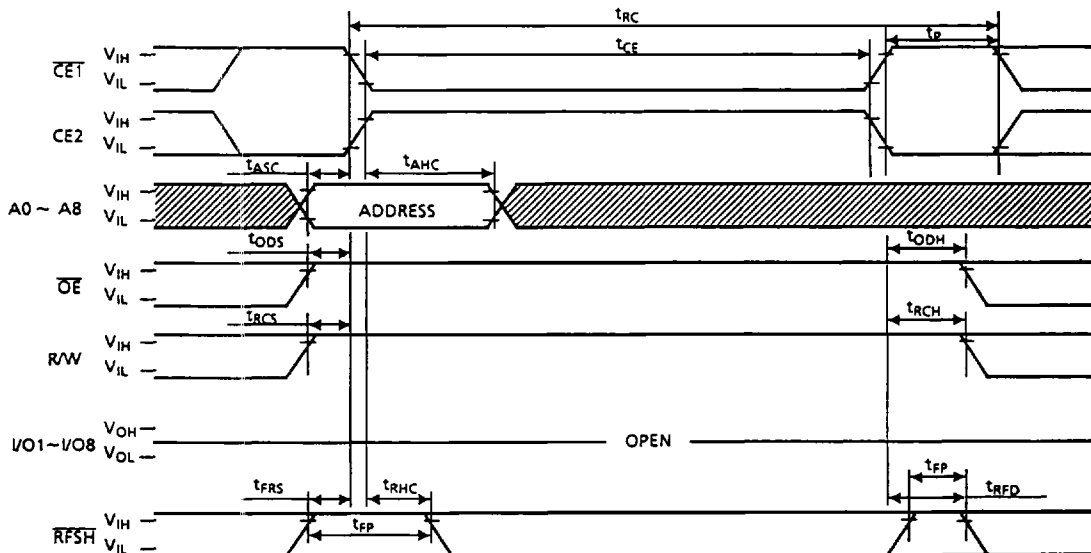
▨ . H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or $\overline{CE2}$) only provided that $\overline{CE2}$ (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

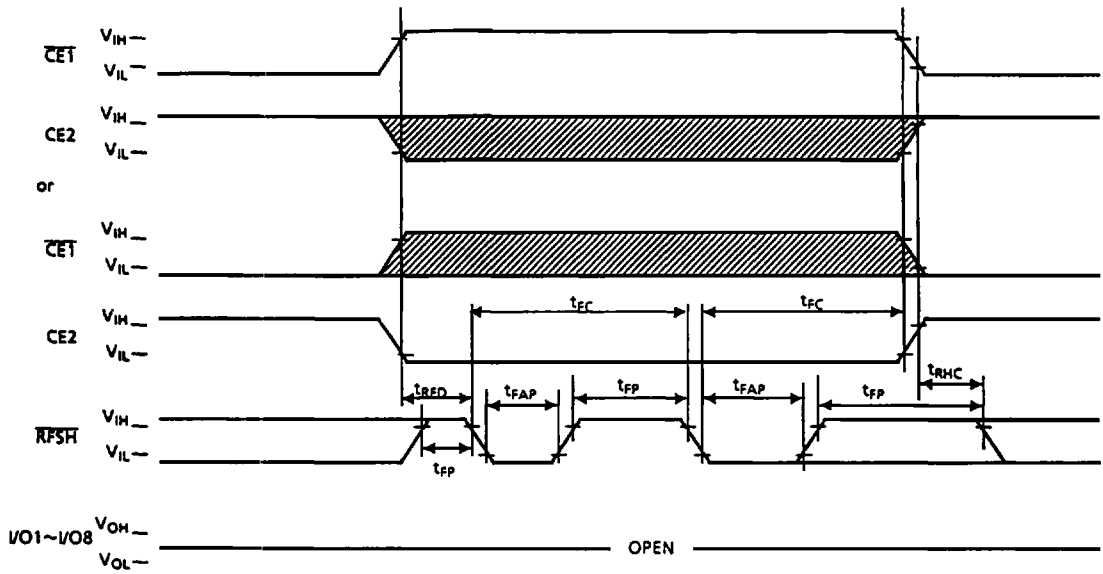


Note : A9 ~ A16 = V_{IH} or V_{IL}

: H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

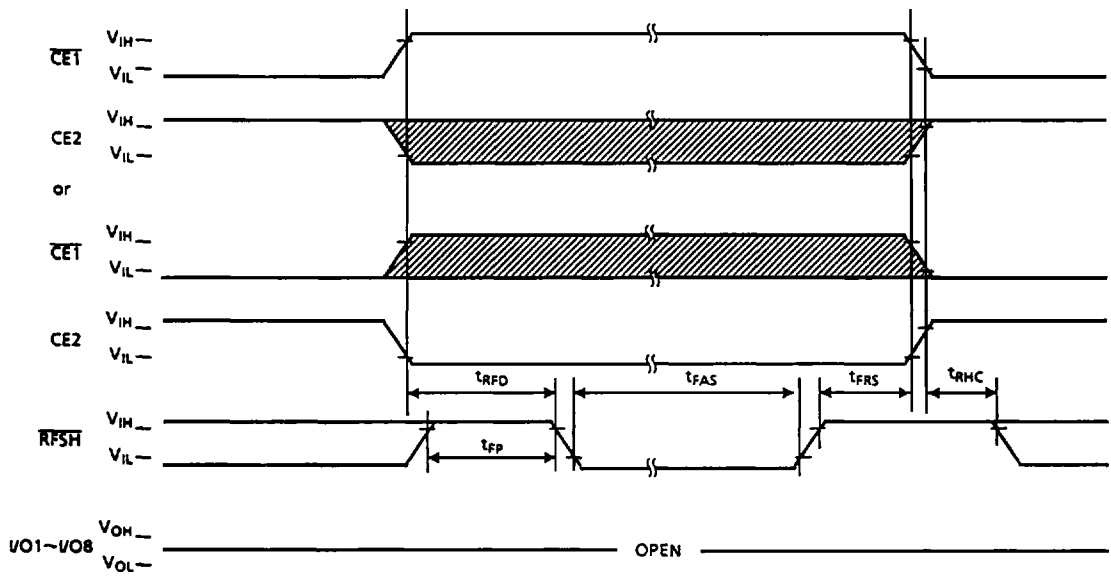
Auto Refresh



Note: \overline{OE} , R/W, A0 ~ A16 = V_{IH} or V_{IL}

: H or L

Self Refresh



Note: \overline{OE} , R/W, A0 ~ A16 = V_{IH} or V_{IL}

: H or L