National Semiconductor

PRELIMINARY
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NS16C2552/NS16C2752 Dual UART with 16-byte/64-byte FIFO's and up to 5 Mbit/s Data Rate

1.0 General Description

The NS16C2552 and NS16C2752 are dual channel Universal Asynchronous Receiver/Transmitter (DUART). The footprint and the functions are compatible to the PC16552D, while new features are added to the UART device. These features include low voltage support, 5V tolerant inputs, enhanced features, enhanced register set, and higher data rate.

The two serial channels are completely independent of each other, except for a common CPU interface and crystal input. On power-up both channels are functionally identical to the PC16552D. Each channel can operate with on-chip transmitter and receiver FIFO's (in FIFO mode).

In the FIFO mode each channel is capable of buffering 16 bytes (for NS16C2552) or 64 bytes (for NS16C2752) of data in both the transmitter and receiver. The receiver FIFO also has additional 3 bits of error data per location. All FIFO control logic is on-chip to minimize system software overhead and maximize system efficiency.

To improve the CPU processing bandwidth, the data transfers between the DUART and the CPU can be done using DMA controller. Signaling for DMA transfers is done through two pins per channel ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$). The $\overline{\text{RXRDY}}$ function is multiplexed on one pin with the $\overline{\text{OUT2}}$ and BAUDOUT functions. The configuration is through Alternate Function Register.

The fundamental function of the UART is converting between parallel and serial data. Serial-to-parallel conversion is done on the UART receiver and parallel-to-serial conversion is done on the transmitter. The CPU can read the complete status of each channel at any time. Status information reported includes the type and condition of the transfer operations being performed by the DUART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The NS16C2552 and NS16C2752 include one programmable baud rate generator for each channel. Each baud rate generator is capable of dividing the clock input by divisors of 1 to (2^{16} - 1), and producing a 16X clock for driving the internal transmitter logic and for receiver sampling circuitry. The NS16C2552 and NS16C2752 have complete MODEM-control capability, and a processor-interrupt system. The interrupts can be programmed by the user to minimize the processing required to handle the communications link.

2.0 Features

- Dual independent UART
- Up to 5 Mbits/s data transfer rate
- 2.97 V to 5.50 V operational Vcc
- 5 V tolerant I/Os in the entire supply voltage range
- Industrial Temperature: -40˚C to 85˚C
- Default registers are identical to the PC16552D
- NS16C2552/NS16C2752 is pin-to-pin compatible to NSC PC16552D, EXAR ST16C2552, XR16C2552, XR 16L2552, and Phillips SC16C2552B
- NS16C2752 is compatible to EXAR XR16L2752, and register compatible to Phillips SC16C752
- Auto Hardware Flow Control (Auto-CTS, Auto-RTS)
- Auto Software Flow Control (Xon, Xoff, and Xon-any)
- Fully programmable character length (5, 6, 7, or 8) with even, odd, or no parity, stop bit
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled and prioritized transmit and receive interrupts
- Complete line status reporting capabilities
- Line break generation and detection
- Internal diagnostic capabilities
  - — Loopback controls for communications link fault isolation
  - — Break, parity, overrun, framing error detection
- Programmable baud generators divide any input clock by 1 to (2^{16} - 1) and generate the 16 X clock
- IrDA v1.0 wireless Infrared encoder/decoder
- DMA operation ($\overline{\text{TXRDY}}$/$\overline{\text{RXRDY}}$)
- Concurrent write to DUART internal register channels 1 and 2
- Multi-function output allows more package functions with fewer I/O pins
- 44-PLCC or 48-TQFP package

NS16C2552/NS16C2752 Dual UART with 16-byte/64-byte FIFO's and up to 5 Mbit/s Data Rate

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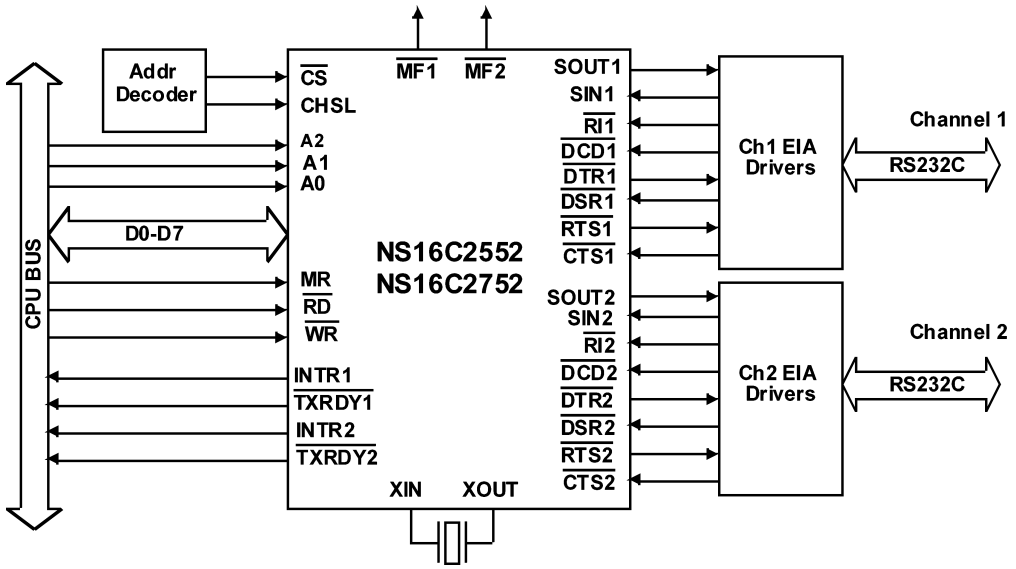
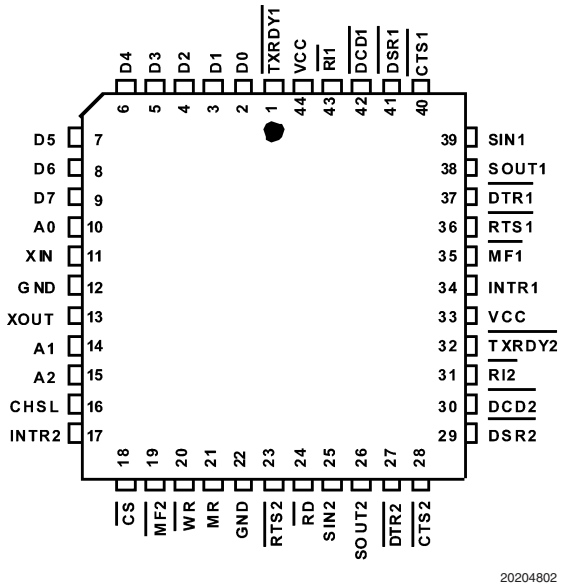
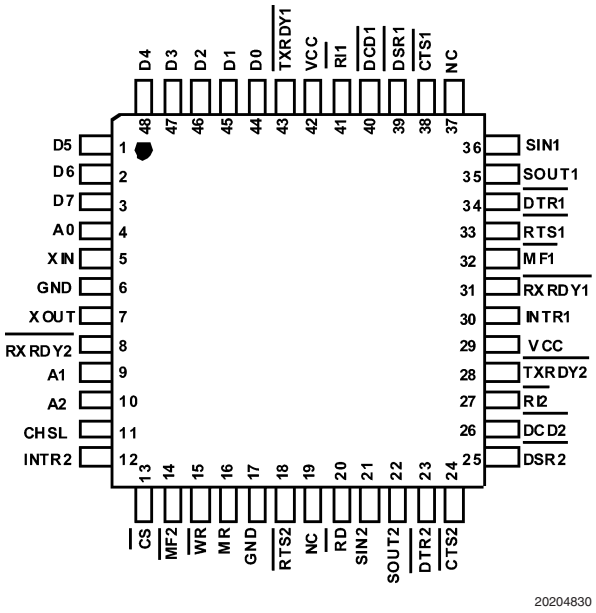
3.0 System Block Diagram



4.0 Connection Diagrams



44–PLCC
Order Number NS16C2552TVA, NS16C2752TVA;
See NS Package Number V44A



48–TQFP
Order Number NS16C2552TVS, NS16C2752TVS;
See NS Package Number VBC48A

5.0 Pin Descriptions

The NS16C2552/NS16C2752 pins are classified into the following interface categories.

- Bus Interface
- Serial I/O Interface
- Clock and Reset
- Power supply and Ground pins

Serial channel number (1 or 2) is designated by a numerical suffix after each pin name. If a numerical suffix (1 or 2) is not associated with the pin name, the information applies to both channels.

The I/O types are as follows:

Type: I	Input
Type: O	Output
Type: IO_Z	TRI-STATE I/O

5.1 PARALLEL BUS INTERFACE

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
D7	IO_Z	9	3	**Data Bus:** Data bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D_7-D_0 Data Bus.
D6		8	2	
D5		7	1	
D4		6	48	
D3		5	47	
D2		4	46	
D1		3	45	
D0		2	44	
A2	I	15	10	**Register Addresses:** Address signals connected to these 3 inputs select a DUART register for the CPU to read from or write to during data transfer. *Table 1* shows the registers and their addresses. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain DUART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches and the Alternate Function Register.
A1		14	9	
A0		10	4	
$\overline{CS}$	I	18	13	**Chip Select:** When $\overline{CS}$ is low, the chip is selected. This enables communication between the DUART and the CPU. Valid chip select should stabilize according to the t_{AW} parameter.
CHSL	I	16	11	**Channel Select:** CHSL directs the address and data information to the selected serial channel. (*Table 1*) 1 = channel 1 is selected. 0 = channel 2 is selected.
$\overline{RD}$	I	24	20	**IO Read:** The register data is placed on the D0 - D7 on the falling edge of $\overline{RD}$. The CPU can read status information or data from the selected DUART register on the rising edge.
$\overline{WR}$	I	20	15	**IO Write:** On the falling edge of $\overline{WR}$, data is placed on the D0 - D7. On the rising edge, the data is latched into the selected DUART register.
$\overline{RXRDY1}$	O	N/A	31	**UART Receive-ready:** The receiver DMA signaling is available through this pin which is a seperate pin on the TQFP package, while on the PLCC package it is available through the $\overline{MF}$ pins (19, 35). When operating in the FIFO mode, the CPU selects one of two types of DMA transfer via FCR[3]. When operating in the 16450 Mode, only DMA mode 0 is available. Mode 0 supports single transfer DMA (and a transfer is usually made between CPU bus cycles). Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the Rx FIFO is empty. Details regarding the active and inactive states of this signal are described in *Section 6.5 FIFO CONTROL REGISTER (FCR)* and *Section 7.9 DMA OPERATION*.
$\overline{RXRDY2}$			8	

5.0 Pin Descriptions (Continued)

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
$\overline{\text{TXRDY1}}$ $\overline{\text{TXRDY2}}$	O	1 32	43 28	**UART Transmit-ready:** Transmitter DMA signaling is available through this pin. When operating in the FIFO mode, the CPU selects one of two types of DMA transfer via FCR[3]. When operating in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA (and a transfer is usually made between CPU bus cycles). Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the Tx FIFO is full. Details regarding the active and inactive states of this signal are described in *Section 6.5 FIFO CONTROL REGISTER (FCR)* and *Section 7.9 DMA OPERATION*.
INTR1 INTR2	O	34 17	30 12	**Interrupt Output:** INTR goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: time-out (FIFO Mode only); Transmitter Holding Register Empty; MODEM Status; and hardware and software flow control. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

5.2 SERIAL IO INTERFACE

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
SOUT1 SOUT2	O	38 26	35 22	**UART Serial Data Out:** UART transmit data output or infrared data output. The SOUT signal is set to logic 1 upon reset or idle in the UART mode when MCR[6]=0. The SOUT signal transitions to logic 0 (idle state of IrDA mode) in the infrared mode when MCR[6]=1. **Note:** SOUT1 and SOUT2 can not be reset to IrDA mode.
SIN1 SIN2	I	39 25	36 21	**UART Serial Data In:** UART receive data input or infrared data input. The SIN should be idling in logic 1 in the UART mode. The SIN should be idling in logic 0 in the infrared mode. The SIN should be pulled high through a 10K resistor if not used.
$\overline{\text{RTS1}}$ $\overline{\text{RTS2}}$	O	36 23	33 18	**UART Request-to-send:** When low, $\overline{\text{RTS}}$ informs the remote link partner that it is ready to receive data. The $\overline{\text{RTS}}$ output signal can be set to an active low by writing "1" to MCR[1]. The RTS output can also be configured in auto hardware flow control based on FIFO trigger level. This pin stays logic 1 upon reset or idle (i.e., between data transfers). Loop mode operation holds this signal in its inactive state.
$\overline{\text{DTR1}}$ $\overline{\text{DTR2}}$	O	37 27	34 23	**UART Data-terminal-ready:** When low, $\overline{\text{DTR}}$ informs the remote link partner that the UART is ready to establish a communications link. The $\overline{\text{DTR}}$ output signal can be set to an active low by writing "1" to MCR[0]. This pin stays at logic 1 upon reset or idle. Loop mode operation holds this signal to its inactive state.
$\overline{\text{CTS1}}$ $\overline{\text{CTS2}}$	I	40 28	38 24	**UART Clear-to-send:** When low, $\overline{\text{CTS}}$ indicates that the remote link partner is ready to receive data. The $\overline{\text{CTS}}$ signal is a modem status input and can be read for the appropriate channel in MSR[4]. This bit reflects the complement of the $\overline{\text{CTS}}$ signal. MSR[0] indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous read of the MSR. $\overline{\text{CTS}}$ can also be configured to perform auto hardware flow control. **Note:** Whenever the $\overline{\text{CTS}}$ bit of the MSR changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

5.0 Pin Descriptions (Continued)

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
$\overline{DSR1}$ $\overline{DSR2}$	I	41 29	39 25	**UART Data-set-ready:** When low, $\overline{DSR}$ indicates that the remote link partner is ready to establish the communications link. The $\overline{DSR}$ signal is a MODEM status input and can be read for the appropriate channel in MSR[5]. This bit reflects the complement of the $\overline{DSR}$ signal. MSR[1] indicates whether the $\overline{DSR}$ input has changed state since the previous read of the MODEM Status Register. **Note:** Whenever the $\overline{DSR}$ bit of the MSR changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{DCD1}$ $\overline{DCD2}$	I	42 30	40 26	**UART Data-carrier-detect:** When low, $\overline{DCD}$ indicates that the data carrier has been detected by the remote link partner. The $\overline{DCD}$ signal is a MODEM status input and can be read for the appropriate channel in MSR[7]. This bit reflects the complement of the $\overline{DCD}$ signal. MSR[3] indicates if the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. **Note:** Whenever the $\overline{DCD}$ bit of the MSR changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{RI1}$ $\overline{RI2}$	I	43 31	41 27	**UART Ring-detector:** When low, $\overline{RI}$ indicates that a telephone ringing is active. The $\overline{RI}$ signal is a MODEM status input and can be read for the appropriate channel in MSR[6]. This bit reflects the complement of the $\overline{RI}$ signal. MSR[2] indicates whether the $\overline{RI}$ input signal has changed state from low to high since the previous reading of the MSR. **Note:** Whenever the $\overline{RI}$ bit of the MSR changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{MF1}$ $\overline{MF2}$	O	35 19	32 14	**UART Multi-function Pin:** $\overline{MF}$ can be programmed for any one of three signal functions $\overline{OUT2}$, $\overline{BAUDOUT}$ or $\overline{RXRDY}$. Bits 2 and 1 of the Alternate Function Register select which output signal will be present on this pin. $\overline{OUT2}$ is the default signal and it is selected immediately after master reset or power-up. The $\overline{OUT2}$ can be set active low by programming bit 3 ($\overline{OUT2}$) of the MCR to a logic 1. A Master Reset operation sets this signal to its inactive (high) state. Loop Mode holds this signal in its inactive state. The $\overline{BAUDOUT}$ signal is the 16X clock output that drives the transmitter and receiver logic of the associated serial channel. This signal is the result of the XIN clock divided by the value in the Divisor Latch Registers. The $\overline{BAUDOUT}$ signal for each channel is internally connected to provide the receiver clock (formerly RCLK on the PC16550D). The $\overline{RXRDY}$ signal can be used to request a DMA transfer of data from the RCVR FIFO. Details regarding the active and inactive states of this signal are described in *Section 6.5 FIFO CONTROL REGISTER (FCR)* and *Section 7.9 DMA OPERATION*.

5.0 Pin Descriptions (Continued)

5.3 CLOCK AND RESET

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
XIN	I	11	5	**External Crystal Input:** XIN input is used in conjunction with XOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal is generated off-chip, then it should drive the baud rate generator through this pin. Refer to *Section 7.1 CLOCK INPUT*.
XOUT	O	13	7	**External Crystal Output:** XOUT output is used in conjunction with XIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal is generated off-chip, then this pin is unused. Refer to *Section 7.1 CLOCK INPUT*.
MR	I	21	16	**Master Reset:** When MR input is high, it clears all the registers including Tx and Rx serial shift registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches). The output signals, such as $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$, INTR, and SOUT are also affected by an active MR input. (Refer to *Table 26* and *Section 7.2 RESET*).

5.4 POWER AND GROUND

Signal Name	Type	PLCC Pin #	TQFP Pin #	Description
VCC	I	33 44	29 42	**V_{CC}:** +2.97V to +5.5V supply.
GND	I	12 22	6 17	**GND:** Device ground reference.
NC	I	N/A	19 37	**No Connection:** These pins are only available on the TQFP package.

6.0 Register Set

There are two identical register sets, one for each channel, in the DUART. All register descriptions in this section apply to the register sets in both channels.

To clarify the descriptions of transmission and receiving operations, the nomenclatures through out this documentation are as follows:

- Frame - Refers to all the bits between Start and Stop.
- Character or word - The payload of a frame, between 5 to 8 bits.
- "!=" - Not equal to.
- Res - Reserved bit.

The address and control pins to register selection is summarized in *Table 1*.

TABLE 1. Basic Register Addresses

	DLAB1	CHSL	A2	A1	A0	Register
CHANNEL1	0	1	0	0	0	Receive Buffer (Read), Transmitter Holding Register (Write)
	0	1	0	0	1	Interrupt Enable
	0	1	0	1	0	Interrupt Identification (Read)
	0	1	0	1	0	FIFO Control (Write)
	x	1	0	1	1	Line Control
	x	1	1	0	0	Modem Control
	x	1	1	0	1	Line Status (Read)
	x	1	1	1	0	Modem Status (Read)
	x	1	1	1	1	Scratchpad
	1	1	0	0	0	Divisor Latch (Least Significant Byte)
	1	1	0	0	1	Divisor Latch (Most Significant Byte)
	1	1	0	1	0	Alternate Function
	DLAB1	**CHSL**	**A2**	**A1**	**A0**	**Register**
CHANNEL2	0	0	0	0	0	Receive Buffer (Read), Transmitter Holding Register (Write)
	0	0	0	0	1	Interrupt Enable
	0	0	0	1	0	Interrupt Identification (Read)
	0	0	0	1	0	FIFO Control (Write)
	x	0	0	1	1	Line Control
	x	0	1	0	0	Modem Control
	x	0	1	0	1	Line Status (Read)
	x	0	1	1	0	Modem Status (Read)
	x	0	1	1	1	Scratchpad
	1	0	0	0	0	Divisor Latch (Least Significant Byte)
	1	0	0	0	1	Divisor Latch (Most Significant Byte)
	1	0	0	1	0	Alternate Function

6.0 Register Set (Continued)

TABLE 2. NS16C2552 Register Summary

Reg Addr A2-A0	RD/ WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Comment
UART 16C550 Compatible Registers (Default Values Upon Reset)										
RBR THR 0x0	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Default		X	X	X	X	X	X	X	X	
IER 0x1	R/W	CTS Int Ena	RTS Int Ena	Xoff Int Ena	Sleep Md Ena	Modem Stat Int Ena	RX Line Stat Int Ena	Tx Empty Int Ena	Rx Data Int Ena	
Default		0	0	0	0	0	0	0	0	LCR[7] = 0
IIR 0x2	R	FIFOs Ena	FIFOs Ena	INT Src Bit 5	INT Src Bit 4	INT Src Bit 3	INT Src Bit 2	INT Src Bit 1	INT Src Bit 0	
Default		0	0	0	0	0	0	0	1	
FCR 0x2	W	RX FIFO Trigger	RX FIFO Trigger	Tx FIFO Trigger (2752)	Tx FIFO Trigger (2752)	DMA Md Ena	Tx FIFO Reset	Rx FIFO Reset	FIFOs Ena	
Default		0	0	0	0	0	0	0	0	
LCR 0x3	R/W	Divisor Ena	Set Tx Break	Set Parity	Even Parity	Parity Ena	Stop Bits	Word Length Bit 1	Word Length Bit 0	
Default		0	0	0	0	0	0	0	0	
MCR 0x4	R/W	Clk Div Sel	IR Md Ena	Xon Any	Internal Loopbk Ena	OUT2	OUT1	RTS Output Control	DTR Output Control	
Default		0	0	0	0	0	0	0	0	
LSR 0x5	R	Rx FIFO Gbl Err	THR & TSR Empty	THR E mpty	Rx Break	Rx Frame Error	Rx Parity Error	Rx Overrun Error	Rx Data Ready	
Default		0	1	1	0	0	0	0	0	LCR != 0xBF
MSR 0x6	R	$\overline{\text{DCD}}$ Input DCD	$\overline{\text{RI}}$ Input RI	$\overline{\text{DSR}}$ Input DSR	$\overline{\text{CTS}}$ Input CTS	Delta $\overline{\text{DCD}}$	Delta $\overline{\text{RI}}$	Delta $\overline{\text{DSR}}$	Delta $\overline{\text{CTS}}$	
Default						0	0	0	0	
SCR 0x7	R/W	SCR Bit 7	SCR Bit 6	SCR Bit 5	SCR Bit 4	SCR Bit 3	SCR Bit 2	SCR Bit 1	SCR Bit 0	
Default		1	1	1	1	1	1	1	1	

6.0 Register Set (Continued)

TABLE 2. NS16C2552 Register Summary (Continued)

Reg Addr A2-A0	RD/ WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Comment
Baud Rate Generator Divisor										
DLL	R/W	DLL	DLL	DLL	DLL	DLL	DLL	DLL	DLL	
0x0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Default		X	X	X	X	X	X	X	X	
DLM	R/W	DLM	DLM	DLM	DLM	DLM	DLM	DLM	DLM	
0x1		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	LCR[7] = 1
Default		X	X	X	X	X	X	X	X	LCR ! 0xBF
AFR	R/W	Rsrvd	Rsrvd	Rsrvd	Rsrvd	Rsrvd	$\overline{\text{RXRDY}}$	$\overline{\text{BAUDOUT}}$	Con-current	
0x2		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Sel	Sel	WR	
Default		0	0	0	0	0	0	0	0	
DREV	R	ID	ID	ID	ID	DREV	DREV	DREV	DREV	LCR[7] = 1
0x0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	LCR != 0xBF
										DLL = 0x00
										DLM = 0x00
Enhanced Registers										
EFR	R/W	Auto	Auto	Special	IER[7:4]	SW	SW	SW Flow	SW	
0x2		CTS Ena	RTS Ena	Char Sel	IIR[5:4] FCR[5:4] MCR[7:5]	Flow Control Bit 3	Flow Control Bit 2	Control Bit 1	Flow Control Bit 0	
Default		0	0	0	0	0	0	0	0	
XON1	R/W	XON1	XON1	XON1	XON1	XON1	XON1	XON1	XON1	
0x4		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Default		0	0	0	0	0	0	0	0	
XON2	R/W	XON2	XON2	XON2	XON2	XON2	XON2	XON2	XON2	LCR = 0xBF
0x5		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Default		0	0	0	0	0	0	0	0	
XOFF1	R/W	XOFF1	XOFF1	XOFF1	XOFF1	XOFF1	XOFF1	XOFF1	XOFF1	
0x6		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Default		0	0	0	0	0	0	0	0	
XOFF2	R/W	XOFF2	XOFF2	XOFF2	XOFF2	XOFF2	XOFF2	XOFF2	XOFF2	
0x7		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Default		0	0	0	0	0	0	0	0	
		Legend	Bit Name Default Value							

The Nomenclature of register descriptions:

- Register name, address, register bit, and value example: FCR 0x2.7:6 = 2'b11 - bits 6 and 7 of FCR are both 1. Alternative description: FCR[7:6] = 2'b11.
- 'b - binary number.
- 'h - hex number.
- 0xNN - hex number.
- n'bN - n is the number of bits; N is the bit value. Example 8'b01010111 = 8'h57 = 0x57.

6.1 RECEIVE BUFFER REGISTER (RBR)

The receiver section contains an 8-bit Receive Shift Register (RSR) and a 16 (or 64)-byte FIFO that can be accessed through Receive Buffer Register (RBR).

6.0 Register Set (Continued)

TABLE 3. RBR (0x0)

Bit	Bit Name	R/W Def	Description
7:0	RBR Data	R 0xXX	**Receive Buffer Register** Rx FIFO data. **Note:** This register value does not change upon MR reset.

6.2 TRANSMIT HOLDING REGISTER (THR)

This register holds the byte-wide transmit data (THR). This is a write-only register.

TABLE 4. THR (0x0)

Bit	Bit Name	R/W Def	Description
7:0	THR Data	W 0xXX	**Transmit Holding Register** Tx FIFO data. **Note:** This register value does not change upon MR reset.

6.3 INTERRUPT ENABLE REGISTER (IER)

This register enables eight types of interrupts for the corresponding serial channel. Each interrupt source can individually activate the interrupt (INTR) output signal. Setting the bits of the IER to a logic 1 unmasks the selected interrupt(s). Similarly, the interrupt can be masked off by resetting bits 0 through 7 of the Interrupt Enable Register (IER). If not desired to be used, masking an interrupt source prevents it from going active in the IIR and activating the INTR output signal. While interrupt sources are masked off, all system functions including the Line Status and MODEM Status still operate in their normal manner. *Table 5* shows the contents of the IER.

TABLE 5. IER (0x1)

Bit	Bit Name	R/W Def	Description
7	CTS Int Ena	R/W 0	**CTS Input Interrupt Enable** 1 = Enable the $\overline{\text{CTS}}$ to generate interrupt at low to high transition. Requires EFR 0x2.4 = 1. 0 = Disable the $\overline{\text{CTS}}$ interrupt (default).
6	RTS Int Ena	R/W 0	**RTS Output Interrupt Enable** 1 = Enable the $\overline{\text{RTS}}$ to generate interrupt at low to high transition. Requires EFR 0x2.4 = 1. 0 = Disable the $\overline{\text{RTS}}$ interrupt (default).
5	Xoff Int Ena	R/W 0	**Xoff Input Interrupt Enable** 1 = Enable the software flow control character Xoff to generate interrupt. Requires EFR 0x2.4 = 1. 0 = Disable the Xoff interrupt (default).
4	Sleep Mode Ena	R/W 0	**Sleep Mode Enable** 1 = Enable the Sleep Mode for the respective channel. Requires EFR 0x2.4 = 1. 0 = Disable Sleep Mode (default).
3	Mdm Stat Int Ena	R/W 0	**Modem Status Interrupt Enable** 1 = Enable the Modem Status Register interrupt. 0 = Disable the Modem Status Register interrupt (default).
2	Rx Line Stat Int Ena	R/W 0	**Receive Line Status Interrupt Enable** An interrupt can be generated when any of the LSR bits 0x5.4:1=1. LSR 0x5.1 generates an interrupt as soon as an overflow frame is received. LSR 0x5.4:2 generate an interrupt when there is read error from FIFO. 1 = Enable the receive line status interrupt. 0 = Disable the receive line status interrupt (default).
1	Tx_Empty Int Ena	R/W 0	**Tx Holding Reg Empty Interrupt Enable** 1 = Enable the interrupt when Tx Holding Register is empty. 0 = Disable the Tx Holding Register from generating interrupt (default).

6.0 Register Set (Continued)

TABLE 5. IER (0x1) (Continued)

Bit	Bit Name	R/W Def	Description
0	Rx_DV Int Ena	R/W 0	**Rx Data Available Interrupt Enable** 1 = Enable the Received Data Available and FIFO mode time-out interrupt. 0 = Disable the Received Data Available interrupt (default).

6.4 INTERRUPT IDENTIFICATION REGISTER (IIR)

In order to provide minimum software overhead during data word transfers, each serial channel of the DUART prioritizes interrupts into seven levels and records these levels in the Interrupt Identification Register. The seven levels of interrupt conditions are listed in *Table 7*. When the CPU reads the IIR, the associated DUART serial channel freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the associated DUART serial channel records new interrupts, but does not change its current indication until the access is complete. *Table 6* shows the contents of the IIR.

TABLE 6. IIR (0x2)

Bit	Bit Name	R/W Def	Description
7:6	FIFOs Ena	R 00	**FIFO Enable Status (FCR 0x2.0)** 2'b11 = Tx and Rx FIFOs enabled. 2'b00 = Tx and Rx FIFOs disabled (default).
5	INT Src 5	R 0	**RTS/CTS Interrupt Status** 1 = $\overline{RTS}$ or $\overline{CTS}$ changed state from low to high. 0 = No change on $\overline{RTS}$ or $\overline{CTS}$ from low to high (default).
4	INT Src 4	R 0	**Xoff or Special Character Interrupt Status** 1 = Receiver detected Xoff or special character. 0 = No Xoff character match (default).
3:1	INT Src 3:1	R 000	**Interrupt Source Status** These three bits indicates the source of a pending interrupt. Refer to *Table 7* for interrupt source and priority.
0	INT Src 0	R 1	**Interrupt Status** 1 = No interrupt is pending (default). 0 = An interrupt is pending and the IIR content may be used as a pointer for the interrupt service routine.

TABLE 7. Interrupt Source and Priority Level

Priority Level	IIR Register Status Bits						Interrupt Source
	5	4	3	2	1	0	
1	0	0	0	1	1	0	LSR
2	0	0	1	1	0	0	RXRDY (Receive data time-out)
3	0	0	0	1	0	0	RXRDY (Receive data ready)
4	0	0	0	0	1	0	TXRDY (Transmit data ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or special character)
7	1	0	0	0	0	0	$\overline{CTS}$, $\overline{RTS}$ change state from low to high
-	0	0	0	0	0	1	None (default)

TABLE 8. Interrupt Sources and Clearing

Interrupt Generation	Interrupt Sources	Interrupt Clearing
LSR	Any bit is set in LSR[4:1] (Break Interrupt, Framing, Rx parity, or overrun error).	Read LSR register. (Interrupt flags and tags are not cleared until the character(s) that generated the interrupt(s) has/have been emptied or cleared.)

6.0 Register Set (Continued)

TABLE 8. Interrupt Sources and Clearing (Continued)

Interrupt Generation	Interrupt Sources	Interrupt Clearing
Rx Trigger	Rx FIFO reached trigger level.	Read FIFO data until FIFO pointer falls below the trigger level.
RXRDY Timer	Time-out in 4-word time plus 12-bit delay time.	Read RBR.
TXRDY	THR empty.	Read from IIR register or a write to THR.
MSR	Any state change in MSR[3:0].	Read from MSR register.
Xoff or Special character	Detection of Xoff or Special character.	Read from IIR register or reception of Xon character (or reception of next character if interrupt is caused by Special character).
CTS	Input pin toggles from logic 0 to 1 during CTS auto flow control mode.	Read from IIR or MSR.
RTS	Output pin toggles from logic 0 to 1 during RTS auto flow control mode.	Read from IIR or MSR.

6.5 FIFO CONTROL REGISTER (FCR)

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the FIFO trigger level, and select the DMA mode.

Mode 0: Mode 0 allows for single transfer in each DMA cycle. When in the 16450 Mode (FCR[0] = 0) or in the FIFO Mode (FCR[0] = 1, FCR[3] = 0) and there is at least one character in the RCVR FIFO or RCVR Buffer Register, the $\overline{\text{RXRDY}}$ pin will go active low. After going active, the $\overline{\text{RXRDY}}$ pin will be inactive when there is no character in the FIFO or Buffer Register.

On The Tx side, $\overline{\text{TXRDY}}$ is active low when XMIT FIFO or XMIT Holding Register is empty. $\overline{\text{TXRDY}}$ returns to high when XMIT FIFO or XMIT holding register is not empty.

Mode 1: Mode 1 allows for multiple transfer or multi-character burst transfer. In the FIFO Mode (FCR[0] = 1, FCR[3] = 1) when the number of characters in the RCVR FIFO equals the trigger threshold level or timeout occurs, the $\overline{\text{RXRDY}}$ goes active low to initiate DMA transfer request. The $\overline{\text{RXRDY}}$ returns high when RCVR FIFO becomes empty.

In the FIFO Mode (FCR[0] = 1, FCR[3] = 1) when there is (1) no character in the XMIT FIFO for NS16C2552, or (2) empty spaces exceed the threshold level for NS16C2752; the $\overline{\text{TXRDY}}$ pin will go active low. This pin will become inactive when the XMIT FIFO is completely full.

TABLE 9. FCR (0x2)

Bit	Bit Name	R/W Def	Description
7:6	Rx FIFO Trig Select	W 00	**Rx FIFO Trigger Select** FCR[6] and FCR[7] are used to designate the interrupt trigger level. When the number of characters in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available Interrupt is activated. This interrupt must be enabled by IER[0]=1. For NS16C2552 with 16-byte FIFO: FCR[7] FCR[6] Rx FIFO Trigger Level 1 1 = 14 1 0 = 8 0 1 = 4 0 0 = 1 (Default) For NS16C2752 with 64-byte FIFO: FCR[7] FCR[6] Rx FIFO Trigger Level 1 1 = 60 1 0 = 56 0 1 = 16 0 0 = 8 (Default) Refer to *Section 7.5 SOFTWARE XON/XOFF FLOW CONTROL* and *Section 7.9 DMA OPERATION* for software flow control using FIFO trigger level.

6.0 Register Set (Continued)

TABLE 9. FCR (0x2) (Continued)

Bit	Bit Name	R/W Def	Description
5:4	Tx FIFO Trig Level Sel	W 00	**Transmit FIFO Trigger Level Selection** The transmit FIFO trigger threshold selection is only available in NS16C2752. When enabled, a transmit interrupt is generated and $\overline{\text{TXRDY}}$ is asserted when the number of empty spaces in the FIFO exceeds the threshold level. For NS16C2752 with 64-byte FIFO: FCR[5] FCR[4] Tx FIFO Trigger Level 1 1 = 56 1 0 = 32 0 1 = 16 0 0 = 8 (Default) Refer to *Section 7.4 TRANSMIT OPERATION* and *Section 7.9 DMA OPERATION* for transmit FIFO descriptions. These two bits are reserved in NS16C2552 and have no impact when they are written to.
3	DMA Mode Select	W 0	**DMA Mode Select** This bit controls the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ initiated DMA transfer mode. 1 = DMA Mode 1. Allows block transfers. Requires FCR 0x2.0=1 (FIFO mode). 0 = DMA Mode 0 (default). Single transfers.
2	Tx FIFO Reset	W 0	**Transmit FIFO Reset** This bit is only active when FCR bit 0 = 1. 1 = Reset XMIT FIFO pointers and all bytes in the XMIT FIFO (the Tx shift register is not cleared and is cleared by MR reset). This bit has the self-clearing capability. 0 = No impact (default). **Note:** Reset pointer will cause the characters in Tx FIFO to be lost.
1	Rx FIFO Reset	W 0	**Receive FIFO Reset** This bit is only active when FCR bit 0 = 1. 1 = Reset RCVR FIFO pointers and all bytes in the RCVR FIFO (the Rx shift register is not cleared and is cleared by MR reset). This bit has the self-clearing capability. 0 = No impact (default). **Note:** Reset pointer will cause the characters in Rx FIFO to be lost.
0	Tx and Rx FIFO Enable	W 0	**Transmit and Receive FIFO Enable** 1 = Enable transmit and receive FIFO. This bit must be set before other FCR bits are written. Otherwise, the FCR bits can not be programmed. 0 = Disable transmit and receive FIFO (default).

6.0 Register Set (Continued)

6.6 LINE CONTROL REGISTER (LCR)

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). This is a read and write register.

TABLE 10. LCR (0x3)

Bit	Bit Name Default	R/W Def	Description
7	Divisor Latch Ena	R/W 0	**Divisor Latch Access Bit (DLAB)** This bit must be set (logic 1) to access the Divisor Latches of the Baud Generator and the Alternate Function Register during a read or write operation. It must be cleared (logic 0) to access any other register. 1 = Enable access to the Divisor Latches of the Baud Generator and the AFR. 0 = Enable access to other registers (default).
6	Tx Break Ena	R/W 0	**Set Tx Break Enable** This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. 1 = Serial output (SOUT) is forced to the Spacing State (break state, logic 0). 0 = The break transmission is disabled (default). Note: This feature enables the CPU to alert a terminal in a computer communication system. If the following sequence is followed, no erroneous or extraneous character will be transmitted because of the break. 1. Load an all 0s, pad character, in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (Transmitter Empty TEMT = 1), and clear break when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to establish the break duration. During the break state, any word left in THR will be shifted out of the register but blocked by SOUT as forced to break state. This word will be lost.
5	Forced Parity Sel	R/W 0	**Tx and Rx Forced Parity Select** When parity is enabled, this bit selects the forced parity format. LCR[5] LCR[4] LCR[3] Parity Select 1 1 1 Force parity to space = 0 1 0 1 Force parity to mark = 1 0 1 1 Even parity 0 0 1 Odd parity X X 0 No parity
4	Even/Odd Parity Sel	R/W 0	**Tx and Rx Even/Odd Parity Select** This bit is only effective when LCR[3]=1. This bit selects even or odd parity format. 1 = Odd parity is transmitted or checked. 0 = Even parity is transmitted or checked (default).
3	Tx/Rx Parity Ena	R/W 0	**Tx and Rx Parity Enable** This bit enables parity generation. 1 = A parity is generated during the data transmission. The receiver checks for parity error of the data received. 0 = No parity (default).

6.0 Register Set (Continued)

TABLE 10. LCR (0x3) (Continued)

Bit	Bit Name Default	R/W Def	Description
2	Tx/Rx Stop-bit Length Sel	R/W 0	**Tx and Rx Stop-bit Length Select** This bit specifies the number of Stop bits transmitted with each serial character. LCR[2] Word Length Sel Stop-bit Length 1 6,7,8 = 2 1 5 = 1.5 0 5,6,7,8 = 1(Default) Stop-bit length is measured in bit time.
1:0	Tx/Rx Word Length Sel	R/W 0	**Tx and Rx Word Length Select** These two bits specify the word length to be transmitted or received. LCR[1] LCR[0] Word Length 1 1 = 8 1 0 = 7 0 1 = 6 0 0 = 5 (Default)

6.0 Register Set (Continued)

6.7 MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). There is a clock divider for each channel. Each is capable of taking a common clock input from DC to 80 MHz and dividing the clock frequency by 1 (default) or 4 depending on the MCR[7] value. The clock divider and the internal clock division flow is shown in *Figure 1*.

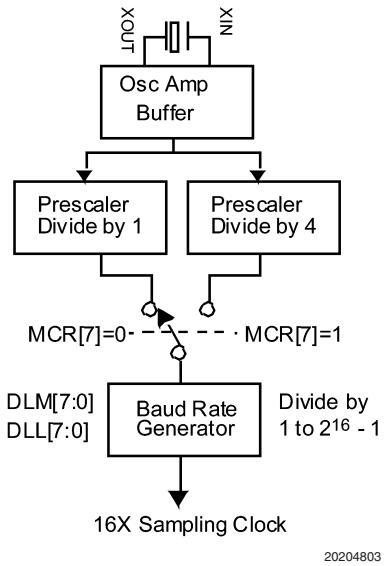


FIGURE 1. Internal Clock Dividers

TABLE 11. MCR (0x4)

Bit	Bit Name	R/W Def	Description
7	Clk Divider Sel	R/W 0	**Clock Divider Select** This bit selects the clock divider from crystal or oscillator input. The divider output connects to the Baud Rate Generator. 1 = Divide XIN frequency by 4. 0 = Divide XIN frequency by 1 (default).
6	IR Mode Sel	R/W 0	**Infrared Encoder/Decoder Select** This bit selects standard modem or IrDA interface. 1 = Infrared IrDA Tx/Rx. The data input and output levels complies to the IrDA infrared interface. The Tx output is at logic 0 during the idle state. 0 = Standard modem Tx/Rx (default).
5	Xon-Any Ena	R/W 0	**Xon-Any Enable** This bit enables Xon-Any feature. 1 = Enable Xon-Any function. When Xon/Xoff flow control is enabled, the transmission resumes when any character is received. The received character is loaded into the Rx FIFO except for Xon or Xoff characters. 0 = Disable Xon-Any function (default).

6.0 Register Set (Continued)

TABLE 11. MCR (0x4) (Continued)

Bit	Bit Name	R/W Def	Description
4	Internal Loopback Ena	R/W 0	**Internal Loopback Enable** This bit provides a local loopback feature for diagnostic testing of the associated serial channel. (Refer to *Section 7.8 INTERNAL LOOPBACK MODE* and *Figure 13*.) 1 = the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is looped back into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four MODEM Control inputs; and the MODEM Control output pins are forced to their inactive state (high). In this diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify transmit and receive data paths of the DUART. In this diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Ena 0 = Normal Tx/Rx operation; loopback disabled (default).
3	OUT2	R/W 0	**Output2** This bit controls the Output 2 ($\overline{OUT2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT2}$ pin as described below. The function of this bit is multiplexed on a single output pin with two other functions: $\overline{BAUDOUT}$ and $\overline{RXDRY}$. The $\overline{OUT2}$ function is the default function of the pin after a master reset. See *Section 6.12 ALTERNATE FUNCTION REGISTER (AFR)* for more information about selecting one of these 3 pin functions. 1 = Force $\overline{OUT2}$ to logic 0. 0 = Force $\overline{OUT2}$ to logic 1 (default).
2	OUT1	R/W 0	**Output1** In normal operation, $\overline{OUT1}$ bit is not available as an output. In internal Loopback Mode (MCR 0x4.4=1) this bit controls the state of the modem input $\overline{RI}$ in the MSR bit 6. 1 = MSR 0x06.6 is at logic 1. 0 = MSR 0x06.6 is at logic 0.
1	RTS Output	R/W 0	**RTS Output Control** This bit controls the $\overline{RTS}$ pin. If modem interface is not used, this output is used as a general purpose output. 1 = Force $\overline{RTS}$ pin to logic 0. 0 = Force $\overline{RTS}$ pin to logic 1(default).
0	DTR Output	R/W 0	**DTR Output Control** This bit controls the $\overline{DTR}$ pin. If modem interface is not used, this output is used as a general purpose output. 1 = Force $\overline{DTR}$ pin to logic 0. 0 = Force $\overline{DTR}$ pin to logic 1(default).

6.0 Register Set (Continued)

6.8 LINE STATUS REGISTER (LSR)

This register provides status information to the CPU concerning the data transfer.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

TABLE 12. LSR (0x5)

Bit	Bit Name	R/W Def	Description
7	Rx FIFO Err	R 0	**Rx FIFO Data Error** This bit is a global Rx FIFO error flag. In the 16450 Mode this bit is 0. 1 = A sum of all error bits in the Rx FIFO. These errors include parity, framing, and break indication in the FIFO data. 0 = No Rx FIFO error (default). **Note:** The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.
6	THR & TSR Empty	R 1	**THR and TSR Empty** This bit is the Transmitter Empty (TEMT) flag. 1 = Whenever the Transmitter Holding Register (THR) (or the Tx FIFO in FIFO mode) and the Transmitter Shift Register (TSR) are both empty (default). 0 = Whenever either the THR (or the Tx FIFO in FIFO mode) or the TSR contains a data word.
5	THR Empty	R 1	**THR Empty** This bit is the Transmitter Holding Register Empty (THRE) flag. In the 16450 mode bit 5 indicates that the associated serial channel is ready to accept a new character for transmission. In addition, this bit causes the DUART to issue an interrupt to the CPU when the Transmit Holding Register Empty interrupt enable is set. 1 = In 16450 mode, whenever a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register, or in FIFO mode when the Tx FIFO is empty (default). 0 = In 16450 mode, this bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In FIFO mode, it is cleared when at least 1 byte is written to the Tx FIFO.
4	Rx Break Interrupt	R 0	**Receive Break Interrupt Indicator** This bit is the Break Interrupt (BI) indicator. 1 = Whenever the received data input is held in the Spacing (logic 0) state for longer than a full frame transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). 0 = No break condition (default). This bit is reset to 0 whenever the CPU reads the contents of the Line Status Register or when the next valid character is loaded into the Receiver Buffer Register. In the FIFO Mode this condition is associated with the particular character in the FIFO it applies to. It is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the Marking (logic 1) state and receives the next valid start bit.

6.0 Register Set (Continued)

TABLE 12. LSR (0x5) (Continued)

Bit	Bit Name	R/W Def	Description
3	Rx Frame Error	R 0	**Framing Error Indicator** This bit is the Framing Error (FE) indicator. 1= Received character did not have a valid Stop bit when the serial channel detects a logic 0 during the first Stop bit time. 0 = No frame error (default). The bit is reset to 0 whenever the CPU reads the contents of the Line Status Register or when the next valid character is loaded into the Receiver Buffer Register. In the FIFO Mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The serial channel will try to resynchronize after a framing error. This assumes that the framing error was due to the next start bit, so it samples this start bit twice and then takes in the data.
2	Rx Parity Error	R 0	**Parity Error Indicator** This bit is the Parity Error (PE) indicator. 1 = Received data word does not have the correct even or odd parity, as selected by the even-parity-select bit during the character Stop bit time when the character has a parity error. 0 = No parity error (default). This bit is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register or when the next valid character is loaded into the Receiver Buffer Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the host when its associated character is at the top of the FIFO.
1	Rx Overrun Error	R 0	**Overrun Error Indicator** This bit is the Overrun Error (OE) indicator. This bit indicates that the next character received was transferred into the Receiver Buffer Register before the CPU could read the previously received character. This transfer overwrites the previous character. It is reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register can be overwritten, but it is not transferred to the FIFO. 1 = Set to a logic 1 during the character stop bit time when the overrun condition exists. 0 = No overrun error (default).
0	Rx Data Ready	R 0	**Receiver Data Indicator** This bit is the receiver Data Ready (DR) indicator. 1 = Whenever a complete incoming character has been received and transferred into the Receiver Buffer Register (RBR) or the FIFO. Bit 0 is reset by reading all of the data in the RBR or the FIFO. 0 = No receive data available (default).

6.0 Register Set (Continued)

6.9 MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. The latter bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

TABLE 13. MSR (0x6)

Bit	Bit Name	R/W Def	Description
7	$\overline{DCD}$ Input Status	R DCD	**$\overline{DCD}$ Input Status** This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. In the loopback mode, this bit is equivalent to the $\overline{OUT2}$ of the MCR. 1 = $\overline{DCD}$ input is logic 0. 0 = $\overline{DCD}$ input is logic 1.
6	$\overline{RI}$ Input Status	R RI	**$\overline{RI}$ Input Status** This bit is the complement of the Ring Indicator ($\overline{RI}$) input. In the loopback mode, this bit is equivalent to $\overline{OUT1}$ of the MCR. 1 = $\overline{RI}$ input is logic 0. 0 = $\overline{RI}$ input is logic 1.
5	$\overline{DSR}$ Input Status	R DSR	**$\overline{DSR}$ Input Status** This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. In the loopback mode, this bit is equivalent to $\overline{DTR}$ in the MCR. 1 = $\overline{DSR}$ input is logic 0. 0 = $\overline{DSR}$ input is logic 1.
4	$\overline{CTS}$ Input Status	R CTS	**$\overline{CTS}$ Input Status** This bit is the complement of the Clear to Send ($\overline{CTS}$) input. In the loopback mode, this bit is equivalent to $\overline{RTS}$ in the MCR. 1 = $\overline{CTS}$ input is logic 0. 0 = $\overline{CTS}$ input is logic 1.
3	DDCD Input Status	R 0	**Delta $\overline{DCD}$ Input Indicator** This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input has changed state since the last read by the host. 1 = $\overline{DCD}$ input has changed state. 0 = $\overline{DCD}$ input has no state change (default). **Note:** Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.
2	Falling Edge RI Indicator	R 0	**Falling Edge $\overline{RI}$ Indicator** This bit is theFalling Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input pin has changed from a logic 0 to 1 since the last read by the host. 1 = $\overline{RI}$ input has changed state from logic 0 to 1. 0 = $\overline{RI}$ input has no state change from 0 to 1 (default).
1	DDSR Input Indicator	R 0	**Delta $\overline{DSR}$ Input Indicator** This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input pin has changed state since the last read by the host. 1 = $\overline{DSR}$ input has changed state from logic 0 to 1. 0 = $\overline{DSR}$ input has no state change from 0 to 1 (default).
0	DCTS Input Indicator	R 0	**Delta $\overline{CTS}$ Input Indicator** This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input pin has changed state since the last time it was read by the host. 1 = $\overline{CTS}$ input has changed state. 0 = $\overline{CTS}$ input has no state change (default).

6.0 Register Set (Continued)

6.10 SCRATCHPAD REGISTER (SCR)

This 8-bit Read/Write Register does not control the serial channel in any way. It is intended as a Scratchpad Register to be used by the programmer to hold data temporarily.

TABLE 14. SCR (0x7)

Bit	Bit Name	R/W Def	Description
7:0	SCR Data	R/W 0xFF	**Scratchpad Register** This 8-bit register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

6.11 PROGRAMMABLE BAUD GENERATOR

The NS16C2552 contains two independently programmable Baud Generators. Each is capable of taking prescaler input and dividing it by any divisor from 1 to 2^{16} -1 (*Figure 1*). The highest input clock frequency recommended with a divisor = 1 is 80MHz. The output frequency of the Baud Generator is 16 X the baud rate, [divisor # = (frequency input) / (baud rate X 16)]. The output of each Baud Generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

TABLE 15. DLL (0x0, LCR[7] = 1, LCR != 0xBF)

Bit	Bit Name	R/W Def	Description
7:0	DLL Data	R/W 0xXX	**Divisor Latch LSB** This 8-bit register holds the least significant byte of the 16-bit baud rate generator divisor. **Note:** This register value does not change upon MR reset.

TABLE 16. DLM (0x1, LCR[7] = 1, LCR != 0xBF)

Bit	Bit Name	R/W Def	Description
7:0	DLM Data	R/W 0xXX	**Divisor Latch MSB** This 8-bit register holds the most significant byte of the 16-bit baud rate generator divisor. **Note:** This register value does not change upon MR reset.

Table 17 provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 18.432 MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is **not** recommended.

TABLE 17. Baud Rate Generation Using 1.8432 MHz Clock with MCR[7]=0

Output Data Baud Rate	Output 16x Clock Divider (dec)	User 16x Clock Divisor (hex)	DLM Program Value (hex)	DLL Program Value (hex)	Data Rate Error (%)
50	2304	900	09	00	0
75	1536	600	06	00	0
150	768	300	03	00	0
300	384	180	01	80	0
600	192	C0	00	C0	0
1200	96	60	00	60	0
2400	48	30	00	30	0
4800	24	18	00	18	0
9600	12	0C	00	0C	0
19,200	6	06	00	06	0
38,400	3	03	00	03	0
115,200	1	01	00	01	0

Note: For baud rates of 250k, 300k, 375k, 500k, 750k and 1.5M using a 24MHz crystal causes minimal error.

6.0 Register Set (Continued)

6.12 ALTERNATE FUNCTION REGISTER (AFR)

This is a read/write register used to select simultaneous write to both register sets and alter MF pin functions.

TABLE 18. AFR (0x2, LCR[7] = 1, LCR != 0xBF)

Bit	Bit Name Default	R/W Def	Description
7:3	Reserved		**Reserved** These bits are set to a logic 0.
2:1	MF Output Sel	R/W 0	**Multi-function Pin Output Select** These select the output signal that will be present on the multi-function pin, $\overline{MF}$. These bits are individually programmable for each channel, so that different signals can be selected on each channel. AFR[2] AFR[1] MF Function 1 1 = Reserved ($\overline{MF}$ output is forced logic 1) 1 0 = $\overline{RXRDY}$ 0 1 = $\overline{BAUDOUT}$ 0 0 = $\overline{OUT2}$ (default)
0	Concurrent Write Ena	R/W 0	**Concurrent Write Enable** 1 = CPU can write concurrently to the same register in both registers sets. This function is intended to reduce the DUART initialization time. It can be used by a CPU when both channels are initialized to the same state. The CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operations. Setting or clearing this bit has no effect on read operations. The user should ensure that the DLAB bit LCR[7] of both channels are in the same state before executing a concurrent write to register addresses 0, 1 and 2. 0 = No concurrent write (default). (No impact on read operations.)

6.13 DEVICE IDENTIFICATION REGISTER (ID)

The device ID for NS16C2552 is 0x03. DLL and DLM should be initialized to 0x00 before reading the ID register. This is a read-only register.

TABLE 19. DREV (0x0, LCR[7]=1, LCR!=0xBF, DLL=DLM=0x00)

Bit	Bit Name	R/W Def	Description
7:4	Device ID	R	**Device ID** Value = 0x3 for NS16C2552; 0x2 for NS16C2752
3:0	Device Rev	R	**Device Revision** Value = 0x1.

6.0 Register Set (Continued)

6.14 ENHANCED FEATURE REGISTER (EFR)

This register enables the enhanced features of the device.

TABLE 20. EFR (0x2, LCR = 0xBF)

Bit	Bit Name Default	R/W Def	Description
7	Auto CTS Flow Ctl Ena	R/W 0	**Automatic CTS Flow Control Enable** 1 = Enable automatic CTS flow control. Data transmission stops when $\overline{CTS}$ input deasserts to logic 1. Data transmission resumes when $\overline{CTS}$ returns to logic 0. 0 = Automatic CTS flow control is disabled (Default)
6	Auto RTS Flow Ctl Ena	R/W 0	**Automatic RTS Flow Control Enable** By setting EFR[6] to logic 1, $\overline{RTS}$ output can be used for hardware flow control. When Auto RTS is selected, an interrupt is generated when the receive FIFO is filled to the programmed trigger level and $\overline{RTS}$ de-asserts to a logic 1. The $\overline{RTS}$ output must be logic 0 before the auto RTS can take effect. $\overline{RTS}$ pin functions as a general purpose output when hardware flow control is disabled. 1 = Enable automatic RTS flow control. 0 = Automatic RTS flow control is disabled (Default)
5	Special Char Det Ena	R/W 0	**Special Character Detect Enable** 1 = Special character detect enabled. The UART compares each incoming received character with data in Xoff-2 register (0x4, LCR = 0xBF). If a match is found, the received data will be transferred to FIFO and IIR[4] is set to indicate the detection of a special character if IER[5] = 1. Bit 0 corresponds with the LSB of the received character. If flow control is set for comparing Xon1, Xoff1 (EFR[1:0] = 10) then flow control and special character work normally; If flow control is set for comparing Xon2, Xoff2 (EFR[1:0]=01) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt if IER[5] is enabled. Special character interrupts are cleared automatically after the next received character. 0 = Special character detect disabled. (Default)
4	Enhanced Fun Bit Ena	R/W 0	**Enhanced Function Bits Enable** This bit enables IER[7:4], FCR[5:4], and MCR [7:5] to be changed. After changing the enhanced bits, EFR[4] can be cleared to logic 0 to latch in the updated values. EFR[4] allows compatibility with the legacy mode software by disabling alteration of the enhanced functions. 1 = Enables writing to IER[7:4], FCR[5:4], and MCR [7:5]. 0 = Disable writing to IER[7:4], FCR[5:4], MCR [7:5] and, latching in updated value. Upon reset, IER[7:4], IIR[5:4], FCR[5:4], and MCR [7:5] are cleared to logic 0. (Default)

6.0 Register Set (Continued)

TABLE 20. EFR (0x2, LCR = 0xBF) (Continued)

Bit	Bit Name Default	R/W Def	Description
3:0	Software Flow Control Sel	R/W 0	**Software Flow Control Select** Single character and dual sequential character software flow control is supported. Combinations of software flow control can be selected by programming the bits.

EFR[3]	EFR[2]	EFR[1]	EFR[0]	Rx Flow Control
1	1	1	1	Rx compares Xon1 & Xon2, Xoff1 & Xoff2
1	0	1	1	Rx compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Rx compares Xon1 or Xon2, Xoff1 or Xoff2
0	0	1	1	Rx compares Xon1 & Xon2, Xoff1 & Xoff2
X	X	1	0	Rx compares Xon1, Xoff1
X	X	0	1	Rx compares Xon2, Xoff2
X	X	0	0	No Rx flow control
0	0	0	0	No Tx & Rx flow control (default)

EFR[3]	EFR[2]	EFR[1]	EFR[0]	Tx Flow Control
1	1	X	X	Tx Xon1 and Xon2, Xoff1 and Xoff2
1	0	X	X	Tx Xon1, Xoff1
0	1	X	X	Tx Xon2, Xoff2
0	0	X	X	No Tx flow control

6.15 SOFTWARE FLOW CONTROL REGISTERS (SFR)

The following four registers are used as programmable software flow control characters.

TABLE 21. Xon1 (0x4, LCR=0xBF)

Bit	Bit Name	R/W Def	Description
7:0	Xon1 Data	R/W 0	**Xon1 Data**

TABLE 22. Xon2 (0x5, LCR=0xBF)

Bit	Bit Name	R/W Def	Description
7:0	Xon2 Data	R/W 0	**Xon2 Data**

TABLE 23. Xoff1 (0x6, LCR=0xBF)

Bit	Bit Name	R/W Def	Description
7:0	Xoff1 Data	R/W 0	**Xoff1 Data**

TABLE 24. Xoff2 (0x7, LCR=0xBF)

Bit	Bit Name	R/W Def	Description
7:0	Xoff2 Data	R/W 0	**Xoff2 Data**

7.0 Operation and Configuration

7.1 CLOCK INPUT

The NS16C2552/2752 has an on-chip oscillator that accepts standard crystal with parallel resonant and fundamental frequency. The generated clock is supplied to both UART channels with the capability range from DC to 24 MHz. The frequency of the clock oscillator is divided by 16 internally, combined with an on-chip programmable clock divider providing the baud rate for data transmission. The divisor is 16-bit with MSB byte in DLM and LSB byte in DLL. The divisor calculation is shown in *Section 6.11 PROGRAMMABLE BAUD GENERATOR*.

The external oscillator circuitry requires two load capacitors, a parallel resistor, and an optional damping resistor. The oscillator circuitry is shown in *Figure 2*.

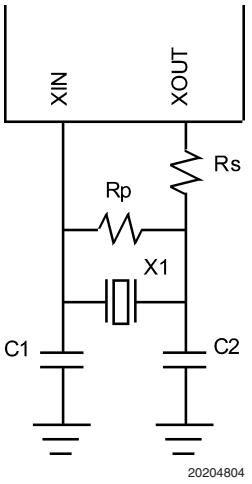


FIGURE 2. Crystal Oscillator Circuitry

The requirement of the crystal is listed in *Table 25*.

TABLE 25. Crystal Component Requirement

Parameter	Value
Crystal Frequency Range	<= 24 MHz
Crystal Type	Parallel resonant
	Fundamental
C1 & C2, Load Capacitance	10 - 22 pF
ESR	20 - 120 Ω
Frequency Stability 0 to 70˚C	100 ppm

The capacitors C1 and C2 are used to adjust the load capacitance on these pins. The total load capacitance (C1, C2 and crystal) must be within a certain range for the NS16C2552/2752 to function properly. The parallel resistor Rp and load resistor Rs are recommended by some crystal vendors. Refer to the vendor's crystal datasheet for details.

Since each channel has a separate programmable clock divider, each channel can have a different baud rate.

The oscillator provides clock to the internal data transmission circuitry, writing and reading from the parallel bus is not affected by the oscillator frequency. For circuits not using the external crystal, the clock input is XIN (*Figure 3*.)

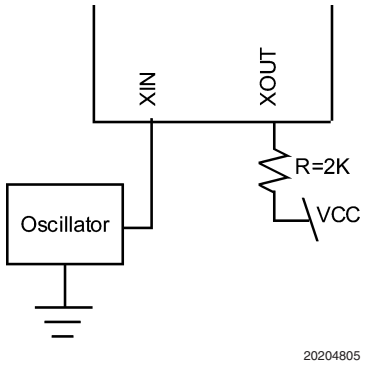


FIGURE 3. Clock Input Circuitry

7.2 RESET

The NS16C2552/2752 has an on-chip power-on reset. An external active high reset can also be applied. The default output state of the device is listed in *Table 26*.

TABLE 26. Output State After Reset

Output	Reset State
SOUT1, SOUT2	Logic 1
$\overline{OUT2}$	Logic 1
$\overline{RTS1}$, $\overline{RTS2}$	Logic 1
$\overline{DTR1}$, $\overline{DTR2}$	Logic 1
INTR1, INTR2	Logic 0
$\overline{TXRDY1}$, $\overline{TXRDY2}$	Logic 0

7.3 RECEIVER OPERATION

Each serial channel consists of an 8-bit Receive Shift Register (RSR) and a 16 (or 64) -byte by 11-bit wide Receive FIFO. The RSR contains a 8-bit Receive Buffer Register (RBR) that is part of the Receive FIFO. The 11-bit wide FIFO contains an 8-bit data field and a 3-bit error flag field. The RSR uses 16X clock as timing source. (*Figure 4*.)

7.0 Operation and Configuration

(Continued)

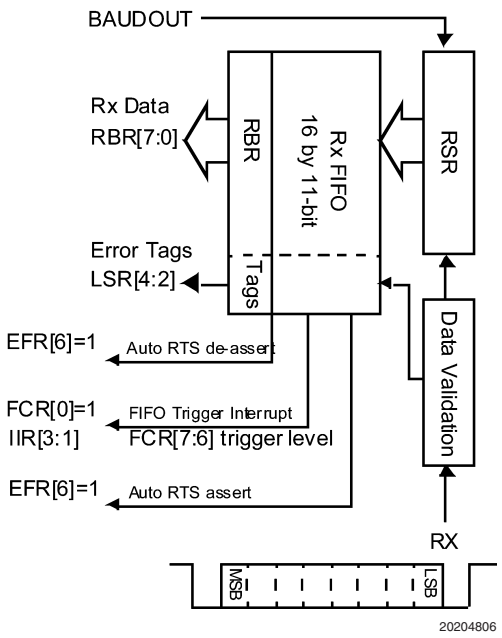


FIGURE 4. Rx FIFO Mode

The RSR operation is described as follows:

1. At the falling edge of the start bit, an internal timer starts counting at 16X clock. At 8th 16X clock, approximately the middle of the start bit, the logic level is sampled. If a logic 0 is detected the start bit is validated.
2. The validation logic continues to detect the remaining data bits and stop bit to ensure the correct framing. If an error is detected, it is reported in LSR[4:2].
3. The data frame is then loaded into the RBR and the Receive FIFO pointer is incremented. The error tags are updated to reflect the status of the character data in RBR. The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the Receive FIFO. It is reset when the Receive FIFO is empty.

7.3.1 Receive in FIFO Mode

Interrupt Mode

In the FIFO mode, FCR[0]=1, RBR can be configured to generate an interrupt after the FIFO pointer reaches a trigger threshold. The interrupt causes CPU host to fetch the Rx character in the FIFO in a burst mode and the transfer number is set by the trigger level. The interrupt is cleared as soon as the number of bytes in the Rx FIFO drops below the trigger level. The Rx FIFO continues to receive new characters, and the interrupt is re-asserted when the character reaches the trigger threshold.

To ensure the data is delivered to the host, a receive data ready time-out interrupt IIR[3] is generated when RBR data is not fetched by the host in 4-word length long (defined in LCR[1:0]) plus 12 bit-time. The RBR interrupt is enabled through IER[0]. This is equivalent of 3.6 to 4.7 frame-time.

The maximum time between a received character and a time-out interrupt will be 147 ms at 300 baud with an 8-bit receive word.

Character delay time is calculated by using the $\overline{\text{BAUDOUT}}$ signal as a clock signal. This makes the delay proportional to the baud rate.

Time-out interrupt is cleared and the timer is reset when the CPU reads one character from the Receive FIFO. When the time-out interrupt is inactive the time-out timer is reset after a new character is received or after the CPU reads the Receive FIFO.

After the first character is read by the host, the next character is loaded into the RBR and the error flags are loaded into LSR[4:2].

DMA Mode

In the FIFO mode, the $\overline{\text{RXRDY}}$ asserts when the character in the Rx FIFO reaches the trigger threshold or timeout occurs. The $\overline{\text{RXRDY}}$ initiates DMA transfer in a burst mode. The $\overline{\text{RXRDY}}$ deasserts when the Rx FIFO is completely emptied and the DMA transfer stops (*Figure 5.*)

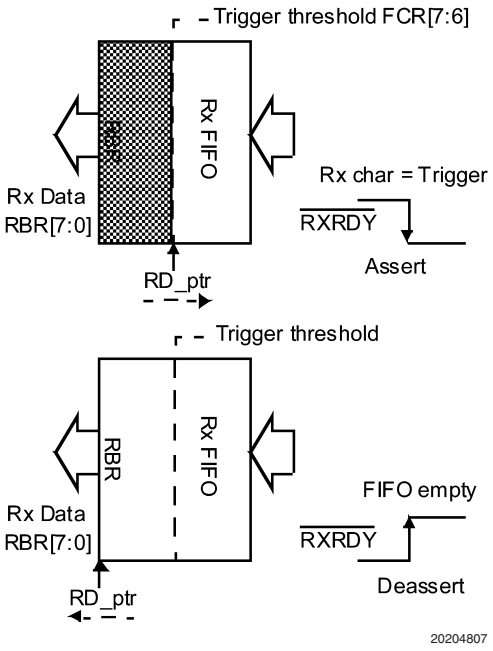


FIGURE 5. RXRDY in DMA Mode 1

7.3.2 Receive in non-FIFO Mode

Interrupt Mode

In the non-FIFO mode, FCR[0]=0, RBR can be configured to generate an IIR Receive Data Available interrupt IIR[2] immediately after the first byte is received. Upon interrupt, the CPU host reads the RBR and clears the interrupt. The interrupt is reasserted when the next character is received. (*Figure 6.*)

7.0 Operation and Configuration

(Continued)

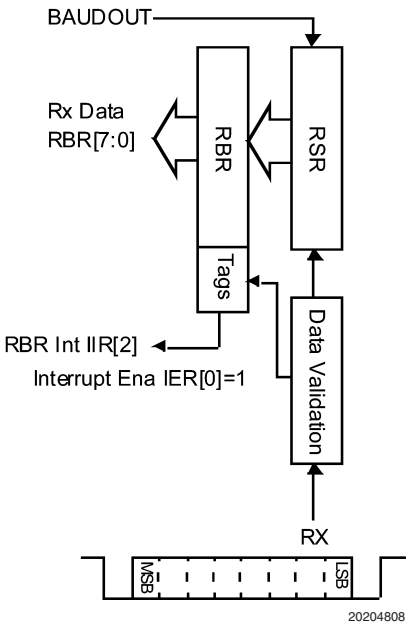


FIGURE 6. Rx Non-FIFO Mode

DMA Mode

In the non-FIFO mode, the presence of a received character in RBR causes the assertion of $\overline{\text{RXRDY}}$ at which point DMA transfer can be initiated. Upon transfer completion $\overline{\text{RXRDY}}$ is deasserted. DMA transfer stops and awaits for the next character. (*Figure 7*.)

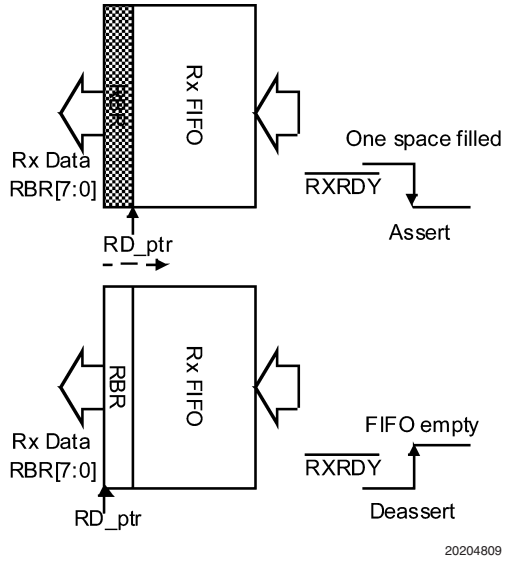


FIGURE 7. RXRDY in DMA Mode 0

7.3.3 Receive Hardware Flow Control

On the line side, $\overline{\text{RTS}}$ signal provides automatic flow control to prevent data overflow in the Receive FIFO. The $\overline{\text{RTS}}$ is used to request remote unit to suspend or resume data transmission. This feature is enabled to suit specific application. The $\overline{\text{RTS}}$ flow control can be enabled by the following steps:

- Enable auto-RTS flow control EFR[6]=1.
- The auto-RTS function is initiated by asserting $\overline{\text{RTS}}$ output pin, MCR[1]=1.

The auto-RTS assertion and deassertion timing is based upon the Rx FIFO trigger level (*Table 27* and *Table 28*).

7.3.4 Receive Flow Control Interrupt

To enable auto RTS interrupt:

- Enable auto RTS flow control EFR[6]=1.
- Enable RTS interrupt IER[6]=1.

An interrupt is generated when RTS pin makes a transition from logic 0 to 1; IIR[5] is set to logic 1.

The receive data ready interrupt (IIR[2]) generation timing is based upon the Rx FIFO trigger level (Table 27 and Table 28).

TABLE 27. Auto-RTS HW Flow Control on NS16C2552

Rx Trigger Level	INTR Pin Activation	RTS Desertion	RTS Assertion
1	1	2	0
4	4	8	1
8	8	14	4
14	14	14	8

TABLE 28. Auto-RTS HW flow Control on NS16C2752

Rx Trigger Level	INTR Pin Activation	RTS Desertion	RTS Assertion
8	8	16	0
16	16	56	8
56	56	60	16
60	60	60	56

7.4 TRANSMIT OPERATION

Each serial channel consists of an 8-bit Transmit Shift Register (TSR) and a 16-byte (or 64-byte) Transmit FIFO. The Transmit FIFO includes a 8-bit Transmit Holding Register (THR). The TSR shifts data out at the 16X internal clock. A bit time is 16 clock periods. The transmitter begins with a start-bit followed by data bits, asserts parity-bit if enabled, and adds the stop-bit(s). The FIFO and TSR status is reported in the LSR[6:5].

The THR is an 8-bit register providing a data interface to the host processor. The host writes transmit data to the THR. The THR is the Transmit FIFO input register in FIFO operation. The FIFO operation can be enabled by FCR[0]=1. During the FIFO operation, the FIFO pointer is incremented pointing to the next FIFO location when a data word is written into the THR.

7.4.1 Transmit in FIFO Mode

Interrupt mode

In the NS16C2752 FIFO mode (FCR[0]=1), when the Tx FIFO empty spaces exceed the threshold level the THR empty flag is set (LSR[5]=1). The THR empty flag generates

7.0 Operation and Configuration

(Continued)

a TXRDY interrupt (IIR[1]=1) when the transmit empty interrupt is enabled (IER[1]=1). Writing to THR or reading from IIR deasserts the interrupt.

There is a two-character hysteresis in interrupt generation. The host needs to service the interrupt by writing at least two characters into the Tx FIFO before the next interrupt can be generated.

The NS16C2552 does not have the FIFO threshold level control. The interrrupt is generated when the FIFO is completely empty.

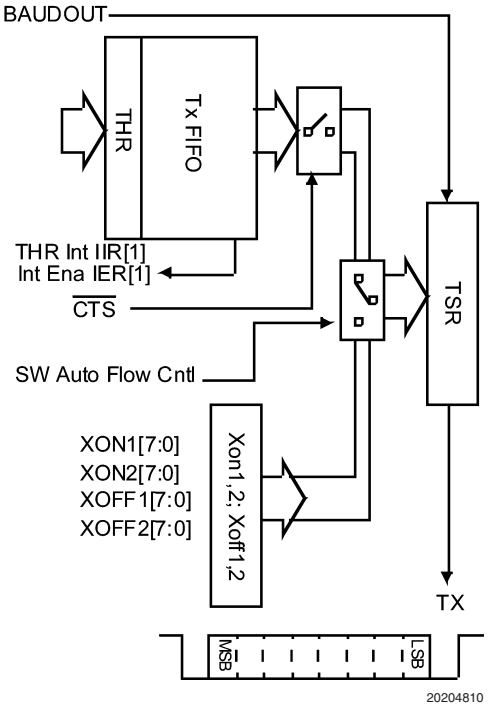


FIGURE 8. Tx FIFO Mode

DMA mode

To fully take advantage of the FIFO buffer, the UART is best operating in DMA mode 1 (FCR[3]=1) when characters are transferred in bursts. The NS16C2752 has a Tx FIFO threshold level control in register FCR[5:4]. The threshold level sets the number of empty spaces in the FIFO and determines when the $\overline{\text{TXRDY}}$ is asserted. If the number of empty spaces in the FIFO exceeds the threshold, the $\overline{\text{TXRDY}}$ asserts initiating DMA transfers to fill the Tx FIFO. When the empty spaces in the Tx FIFO becomes zero (i.e., FIFO is full), the $\overline{\text{TXRDY}}$ deasserts and the DMA transfer stops. $\overline{\text{TXRDY}}$ reasserts when empty space exceeds the set threshold, starting a new DMA transfer cycle. (*Figure 9.*)

The NS16C2552 does not have the FIFO threshold level control. The $\overline{\text{TXRDY}}$ is asserted when FIFO is empty and deasserted when FIFO is full. It is equivalent of having trigger threshold set at 16 empty spaces.

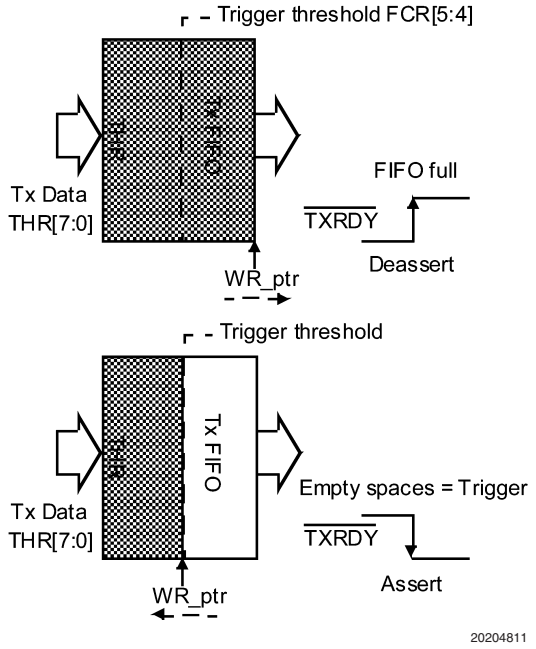


FIGURE 9. TXRDY in DMA Mode 1

7.4.2 Transmit in non-FIFO Mode

Interrupt Mode

The THR empty flag LSR[5] is set when a data word is transferred to the TSR. THR flag can generate a transmit empty interrupt IIR[1] enabled by IER[1]. The TSR flag LSR[6] is set when TSR becomes empty. The host CPU may write one character into the THR and wait for the next IIR[1] interrupt. (*Figure 10.*)

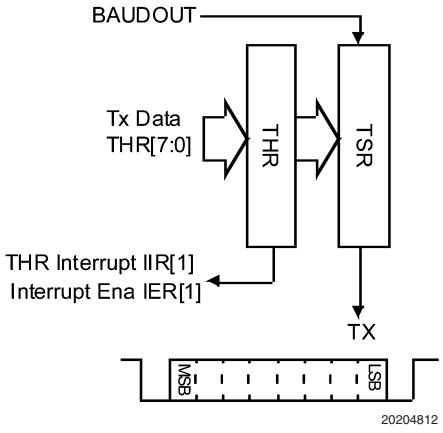


FIGURE 10. Tx Non-FIFO Mode

DMA mode

In the DMA single transfer (mode 0), $\overline{\text{TXRDY}}$ asserts when FIFO is empty initiating one DMA transfer and deasserts when a character is written into the FIFO. (*Figure 11.*)

7.0 Operation and Configuration

(Continued)

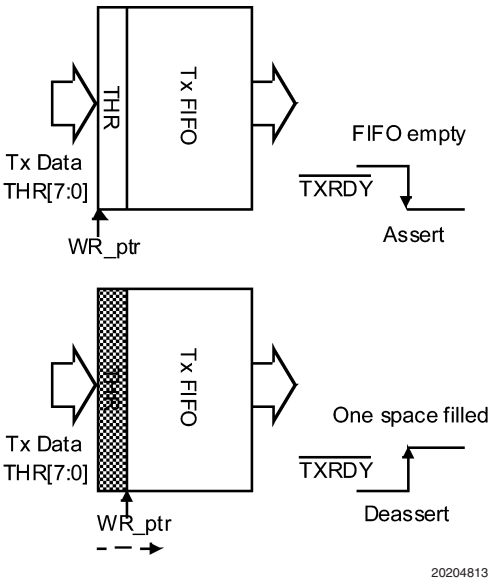


FIGURE 11. TXRDY in DMA Mode 0

7.4.3 Transmit Hardware Flow Control

$\overline{CTS}$ is a flow control input used to prevent remote receiver FIFO data overflow. The $\overline{CTS}$ input is monitored to suspend/resume the local transmitter. The automatic CTS flow control can be enabled to suit specific application.

- Enable auto CTS flow control EFR[7]=1.

7.4.4 Transmit Flow Control Interrupt

- Enable auto CTS flow control EFR[7]=1.
- Enable CTS interrupt IER[7]=1.

An interrupt is generated when $\overline{CTS}$ pin is de-asserted (logic 1). IIR[5] is set to logic 1. The transmitter suspends transmission as soon as the stop bit is shifted out. Transmission is resumed after the $\overline{CTS}$ pin is asserted logic 0, indicating remote receiver is ready to accept data word.

7.5 SOFTWARE XON/XOFF FLOW CONTROL

Software flow control uses programmed Xon or Xoff characters to enable the transmit/receive flow control. The receiver compares one or two sequentially received data words. If the received character(s) match the programmed values, the transmitter suspends operation as soon as the current transmitting frame is completed. When a match occurs, the Xoff (if enabled via IER[5]) flag is set and an interrupt is generated. Following a transmission suspension, the UART monitors the receive data stream for an Xon character. When a match is found, the transmission resumes and the IIR[4] flag clears.

Upon reset, the Xon/Xoff characters are cleared to logic 0. The user may write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the UART compares two consecutively received characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, and Xoff2) and controls transmission accordingly. Under the above described flow control mechanisms, flow control characters are not placed in the user accessible Rx data buffer or FIFO.

During the flow control operation, when Receive FIFO pointer reaches the upper trigger level, the UART automatically transmits Xoff1 and Xoff 2 messages via the serial TX line output to the remote modem. When Receive FIFO pointer position matches the lower trigger level, the UART automatically transmits Xon1 and Xon2 characters.

Care should be taken when designing the software flow control section of the driver. In the case where a local UART is transmitting and the remote UART initiates flow control, an Xoff character is sent by the remote UART.

Upon receipt the local UART ceases to transmit until such time as the remote UART FIFO has been drained sufficiently and it signals that it can accept further data by sending an Xon character to the local UART.

There is a corner case in which the receipt of an Xoff by the local UART can occur just after it has sent the last character of a data transfer and is ready to close the transmission. If in so doing the driver disables the local UART, it may not receive the corresponding XON and thus can remain in a flow-controlled state. This will persist even when the UART is re-enabled for a succeeding transmission creating a lock-up situation.

To resolve this lock-up issue, the driver should implement a delay before shutting down the local transmitter at the end of a data transfer. This delay time should be equal to the transmission time of four characters PLUS the latency required to drain the RX FIFO on the remote side of the connection. This will allow the remote modem to send an Xon character and for it to be received before the local transmitter shuts down.

TABLE 29. Xon/Xoff SW Flow Control on NS16C2552

Rx Trigge Level	INTR Pin Activation	Xoff Char Sent	Xon Char Sent
1	1	1	0
4	4	4	1
8	8	8	4
14	14	14	8

TABLE 30. Xon/Xoff SW Flow Control on NS16C2752

Rx Trigger Level	INTR Pin Activation	Xoff Char Sent	Xon Char Sent
8	8	8	0
16	16	16	8
56	56	56	16
60	60	60	56

7.6 SPECIAL CHARACTER DETECT

UART can detect an 8-bit special character if EFR[5]=1. When special character detect mode is enabled, the UART compares each received character with Xoff2. If a match is found, Xoff2 is loaded into the FIFO along with the normal received data and IIR[4] is flagged to logic 1.

The Xon and Xoff word length is programmable between 5 and 8 bits depending on LCR[1:0] with the LSB bit mapped to bit 0. The same word length is used for special character comparison.

7.0 Operation and Configuration

(Continued)

7.7 SLEEP MODE

To reduce power consumption, NS16C2552/2752 has a per channel sleep mode when channel is not being used. The sleep mode requires following conditions to be met:

- Sleep mode of the respective channel is enabled (IER[4]=1).
- No pending interrupt for the respective channel (IIR[0]=1).
- Divisor is a non-zero value (DLL or DLM != 0x00).
- Modem inputs are not toggling (MSR[3:0]=0).
- Receiver input is idling at logic 1.

The channel wakes up from sleep mode and returns to normal operation when one of the following conditions is met:

- Start bit falling edge (logic 1 to 0) is detected on receiver.
- A character is loaded into the THR or Tx FIFO
- A state change on any of the modem interface inputs, $\overline{DTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$.

Following the awakening, the channel can fall back into the sleep mode when all interrupt conditions are serviced and cleared. If channel is awakened by the modem line inputs, reading the MSR resets the line inputs.

Following the awakening, the interrupts from the respective channel has to be serviced and cleared before re-entering into the sleep mode. The NS16C2552/2752 sleep mode can be disabled by IER[4]=0.

7.8 INTERNAL LOOPBACK MODE

NS16C2552 incorporates internal loopback path for design validation and diagnostic trouble shooting. In the loopback mode, the transmitted data is looped from the transmit shift register output to the receive shift register input internally. The system receives its transmitted data. The loopback mode is enabled by MCR[4]=1 (*Figure 13*).

In the loopback mode, Tx pin is held at logic 1 or mark condition while $\overline{RTS}$ and $\overline{DTR}$ are de-asserted and $\overline{CTS}$, $\overline{DRS}$, $\overline{CD}$, and $\overline{RI}$ inputs are ignored. Note that Rx input must be held at logic 1 during the loopback test. This is to prevent false start bit detection upon exiting the loopback mode. $\overline{RTS}$ and $\overline{CTS}$ are disabled during the test.

7.9 DMA OPERATION

LSR[6:5] provide status of the transmit FIFO and LSR[0] provides the receive FIFO status. User may read the LSR status bits to initiate and stop data transfers.

More efficient direct memory access (DMA) transfers can be setup using the $\overline{RXRDY}$ and $\overline{TXRDY}$ signals. The DMA transfers are asserted between the CPU cycles and saves CPU processing bandwidth. In mode 0, (FCR[3]=0), each assertion of $\overline{RXRDY}$ and $\overline{TXRDY}$ will cause a single transfer. Note that the user should verify the interface to make sure the signaling is compatible with the DMA controller.

With built-in transmit and receive FIFO buffers it allows data to be transferred in blocks (mode 1) and it is ideal for more efficient DMA operation that further saves the CPU processing bandwidth.

To enable the DMA mode 1, FCR[3]=1. The DMA Rx FIFO reading is controlled by $\overline{RXRDY}$. When FIFO data is filled to the trigger level, $\overline{RXRDY}$ asserts and the DMA burst transfer begins removing characters from Rx FIFO. The DMA transfer stops when Rx FIFO is empty and $\overline{RXRDY}$ deasserts.

The DMA transmit operation is controlled by $\overline{TXRDY}$ and is different between the NS16C2552 and NS16C2752. On the NS16C2552, the DMA operation is initiated when transmit FIFO becomes empty and $\overline{TXRDY}$ is asserted. The DMA controller fills the Tx FIFO and the filling stops when FIFO is full and $\overline{TXRDY}$ is deasserted.

On the NS16C2752, the DMA transfer starts when the Tx FIFO empty space exceeds the threshold set in FCR[5:4] and $\overline{TXRDY}$ asserts. The transfer stops when Tx FIFO is full and $\overline{TXRDY}$ desserts. The threshold setting gives CPU more time to arbitrate and relinquish bus control to DMA controller providing higher bus efficiency.

7.10 INFRARED MODE

NS16C2552/2752 also integrates an IrDA version 1.0 compatible infrared encoder and decoder. The infrared mode is enabled by MCR[6]=1.

In the infrared mode, the SOUT idles at logic 0. During data transmission, the encoder transmits a 3/16 bit wide pulse for each logic 0. With shortened transmitter-on light pulse, power saving is achieved.

On the receiving end, each light pulse detected translates to a logic 0, active low (*Figure 12*.)

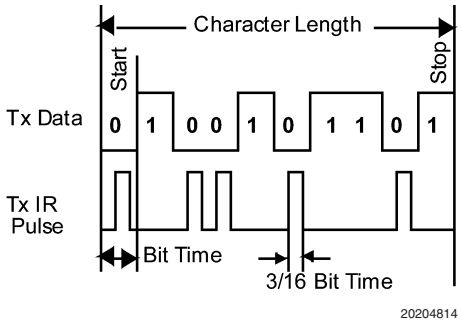


FIGURE 12. IrDA Data Transmission

7.0 Operation and Configuration (Continued)

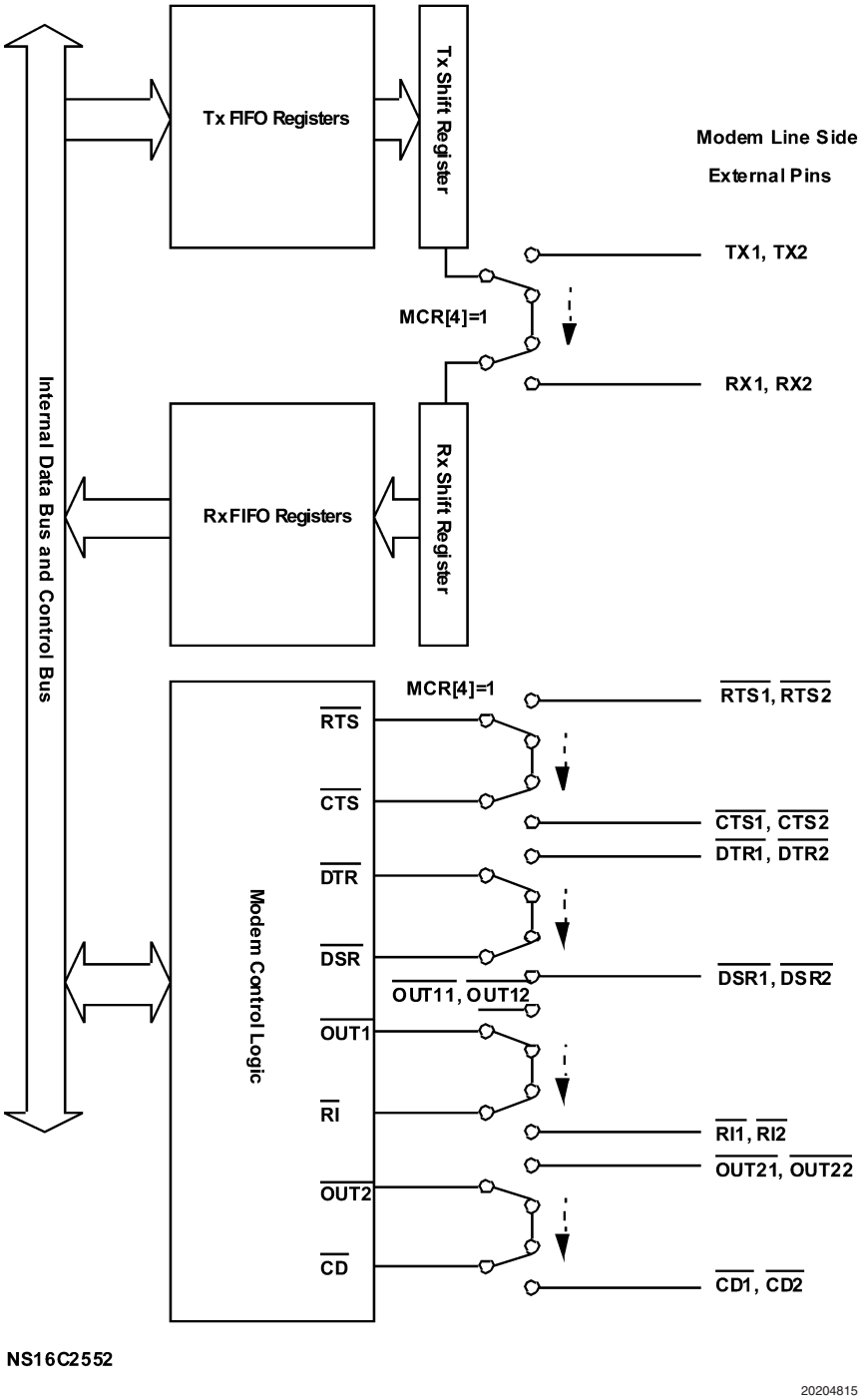


FIGURE 13. Internal Loopback Functional Diagram

8.0 Design Notes

8.1 DEBUGGING HINTS

Although the UART device is fairly straight forward, there are cases that when device does not behave as expected. The normal trouble shooting steps should include the following.

1. Check power supply voltage and make sure it is within the operating range.
2. Check device pin connections against the datasheet pin list.
3. Check an unpopulated printed circuit board (PCB) against the schematic diagram for any shorts.
4. Check the device clock input. For oscillator input, the scope probe can be attached to Xin to verify the clock voltage swing and frequency. For crystal connection, attach the scope probe to Xout to check for the oscillation frequency.
5. Reset should be active high and normally low.
6. Use internal loopback mode to test the CPU host interface. If loopback mode is not working, check the CPU interface timing including read and write bus timing.
7. If loopback mode is getting the correct data, check serial data output and input. The transmit and receive data may be looped back externally to verify the data path integrity.

8.2 CLOCK FREQUENCY ACCURACY

In the UART transmission, the transmitter clock and the receive clock are running in two different clock domains (unlike in some communication interface that the received clock is a copy of the transmitter clock by sharing the same clock or by performing clock-data-recovery). Not only the local oscillator frequency, but also the clock divisor may introduce error in between the transmitter and receiver's baud rate. The question is how much error can be tolerated and does not cause data error?

The UART receiver has an internal sampling clock that is 16X the data rate. The sampling clock allows data to be sampled at the 6/16 to 7/16 point of each bit. The following is an example of a 8-bit data packet with a start, a parity, and one stop bit. (*Figure 14*)

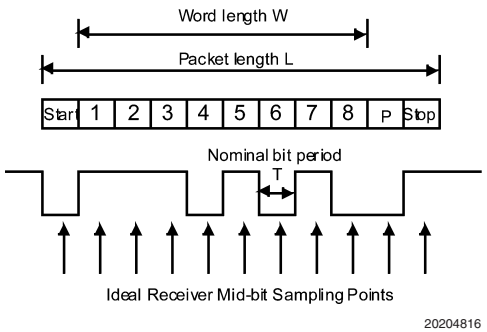


FIGURE 14. Nominal Mid-bit Sampling

If a receiver baud rate generator deviates from the nominal baud rate by Δf, where $1/\Delta f = \Delta T$, the first sampling point will deviate from the nominal sample point by $0.5\Delta T$. Consequently, the second sampling point will deviate by $1.5\Delta T$, 3rd will deviate by $2.5\Delta T$, and the last bit of a packet with L length (in number of bits) will deviate by

$(L - 0.5) \times \Delta T$

In this example, L=11, so that the last bit will deviate by $(11 - 0.5) \times \Delta T = 10.5\Delta T$(*Figure 15*)

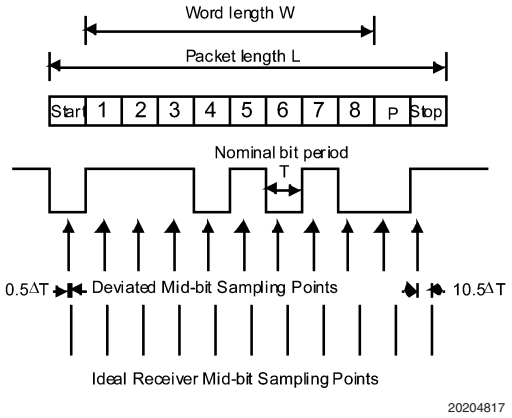


FIGURE 15. Deviated Baud Rate Sampling

Giving some margin for sampling error due to metastability and jitter assuming that the bit period deviation can not be more than 6/16 the bit time (i.e., the worst case), 0.375T. So that

$(L - 0.5) \times \Delta T < 0.375T$

for the receiver to correctly recover the transmitted data. Reform the equation

$\Delta T < 0.375T / (L - 0.5)$

Using the same example of 11-bit packet (L = 11), at 9600 baud, f = 9600, the sampling clock rate is f (i.e., one sample per period) and the bit period is

$T = 1 / f$

$\Delta T < 0.375T / (L - 0.5) = 0.375 / (f \times (L - 0.5))$

$\Delta T < 0.375 / (9600 \times 10.5) = 3.7 \times 10^{-6}$ (sec) or 3.7 µs.

The percentage of the deviation from nominal bit period has to be less than

$\Delta T / T = (0.375 / (f \times (L - 0.5)) \times f = 0.375 / L - 0.5)$

$\Delta T / T = 3.7 \times 10^{-6} \times 9600 = 3.6\%$

From the above example, the error percentage increases with longer packet length (i.e., larger L). The best case is packet with word length 5, a start bit and a stop bit (L = 7) that is most tolerant to error.

$\Delta T / T = 0.375 / (L - 0.5) = 0.375 / 6.5 = 5.8\%$

The worst case is packet with word length 8, a start bit, a parity bit, and two stop bits (L = 12) that is least tolerant to error.

$\Delta T / T = 0.375 / L - 0.5) = 0.375 / 11.5 = 3.2\%$

8.3 CRYSTAL REQUIREMENTS

The crystal used should meet the following requirements.

1. AT cut with parallel resonance.
2. Fundamental oscillation mode between 1 to 24 MHz.
3. Frequency tolerance and drift is well within the UART application requirements, and they are not a concern.

8.0 Design Notes (Continued)

4. The load capacitance of the crystal should match the load capacitance of the oscillator circuitry seen by the crystal. Under the AC conditions, the oscillator load capacitance is a lump sum of parasitic capacitance and external capacitors. The capacitances connecting to oscillator input and output are in series seen by the crystal. (*Figure 16*.) External capacitors, C1 and C2, are not required to be very accurate. The best practice to follow crystal manufacturer's recommendation for the load capacitance value.

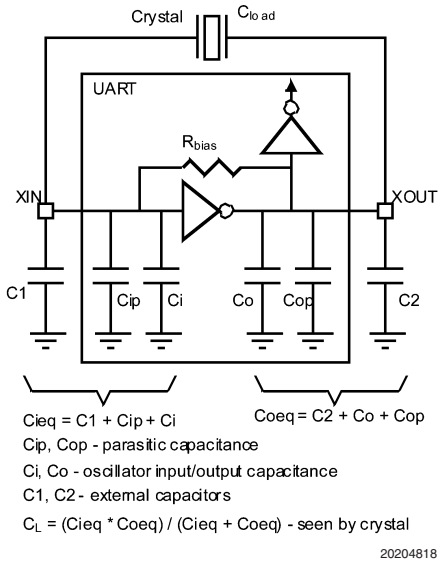


FIGURE 16. Crystal Oscillator Circuit

It should be noted that the parasitic capacitance also include printed circuit board traces. The circuit board traces connecting to the crystal should be kept as short as possible.

8.4 CONFIGURATION EXAMPLES

8.4.1 Set Baud Rate

Set divisor values to DIV_L and DIV_M.

- LCR 0x03.7 = 1
- DLL 0x00.7:0 = DIV_L
- DLM 0x01.7:0 = DIV_M
- LCR 0x03.7 = 0

8.4.2 Configure Prescaler Output

Set prescaler output to XIN divide by 4.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 1
- LCR 0x03.7:0 = 0
- MCR 0x04.7 = 1
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 0 (optional)
- LCR 0x03.7:0 = temp

Set prescaler output to XIN divide by 1.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 1
- LCR 0x03.7:0 = 0
- MCR 0x04.7 = 0
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 0 (optional)
- LCR 0x03.7:0 = temp

8.4.3 Set Xon and Xoff flow control

Set Xon1, Xoff1 to VAL1 and VAL2.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- Xon1 0x04.7:0 = VAL1
- Xoff1 0x06.7:0 = VAL2
- LCR 0x03.7:0 = temp

Set Xon2, Xoff2 to VAL1 and VAL2.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- Xon2 0x05.7:0 = VAL1
- Xoff2 0x07.7:0 = VAL2
- LCR 0x03.7:0 = temp

8.4.4 Set Software Flow Control

Set software flow control mode to VAL.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.3:0 = VAL
- LCR 0x03.7:0 = temp

8.4.5 Configure Tx/Rx FIFO Threshold

Set Tx (2752) and Rx FIFO thresholds to VAL.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 1
- LCR 0x03.7:0 = 0
- FCR 0x02.7:0 = VAL
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.4 = 0 (optional)
- LCR 0x03.7:0 = temp

8.4.6 Tx and Rx Hardware Flow Control

Configure auto RTS and CTS flow controls, enable RTS and CTS interrupts, and assert RTS.

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0xBF
- EFR 0x02.7:6 = 2b'11
- EFR 0x02.4 = 1
- LCR 0x03.7:0 = 0
- IER 0x01.7:6 = 2b'11
- MCR 0x04.1 = 1
- LCR 0x03.7:0 = temp

8.4.7 Tx and Rx DMA Control

Configure Tx and Rx in FIFO mode DMA transfers using the threshold in FCR[7:4].

- Save LCR 0x03.7:0 in temp
- LCR 0x03.7:0 = 0
- FCR 0x02.0 = 1

8.0 Design Notes (Continued)

- FCR 0x02.3 = 1
- LCR 0x03.7:0 = temp

8.5 DIFFERENCES BETWEEN THE PC16552D AND NS16C2552/2752

The following are differences between the versions of UART that helps user to identify the feature differences.

TABLE 31. Differences among the UART products

Features	PC16552D	NS16C2552	NS16C2752
Tx and Rx FIFO sizes	16-byte	16-byte	64-byte
Supply voltage	4.5V to 5.5V	2.97V to 5.5V	2.97V to 5.5V
Highest baud rate	1.5Mbps	5.0Mbps	5.0Mbps
Highest clock input frequency	24MHz	80MHz	80MHz
Operating temperature	0 - 70˚C	-40 to 85˚C	-40 to 85˚C
Enhanced Register Set	No	Yes	Yes
Sleep mode IER[4]	No	Yes	Yes
Xon, Xoff, and Xon-Any software auto flow control	No	Yes	Yes
CTS and RTS hardware auto flow control	No	Yes	Yes
Interrupt source ID in IIR	3-bit	5-bit	5-bit
Tx FIFO trigger level select FCR[5:4]	1 level	1 level	4 levels
IrDA v1.0 mode MCR[6]	No	Yes	Yes
Clock divisor 1 or 4 select MCR[7]	No	Yes	Yes

8.6 NOTES ON TX FIFO OF NS16C2752

Notes on interrupt assertion and deassertion.

1. To avoid frequent interrupt request generation, there is a hysteresis of two characters. When the transmit FIFO threshold is enabled and the number of empty spaces reaches the threshold, a THR empty interrupt is generated requesting the CPU to fill the transmit FIFO. The host has to fill at least two characters in the Tx FIFO before another THR empty interrupt can be generated.

   The DMA request $\overline{\text{TXRDY}}$ works differently. When the number of empty spaces exceeds the threshold, $\overline{\text{TXRDY}}$ asserts initiating the DMA transfer. The $\overline{\text{TXRDY}}$ deasserts when the transmit FIFO is full.
2. When the number of empty spaces reaches the threshold level, an interrupt is generated. If the host does not fill the FIFO, the interrupt will remain asserted until the host writes to the THR or reads from IIR.
3. When the number of empty spaces reaches the threshold level, an interrupt is generated. If the host reads the IIR but does not fill the Tx FIFO, the INTR is deasserted. However, if the host still does not fill the Tx FIFO, the FIFO becomes empty. The THR empty interrupt is not generated because the host has not written to the Tx FIFO and the interrupt service is not complete.
4. When the number of empty spaces reaches the threshold level, a THR empty interrupt is generated. If the host writes at least one character into the Tx FIFO, the interrupt is serviced and the THR empty flag is deasserted. Subsequently, if the host fails to fill the FIFO before it reaches empty, a THR empty interrupt will be asserted.
5. Reset Tx FIFO causes a THR empty interrupt.

9.0 Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Temperature	–40˚C to +85˚C
Storage Temperature	–65˚C to +150˚C
All Input or Output Voltages with respect to V_{ss}	–0.5V to +6.5V
Power Dissipation	250mW
ESD Rating HBM, 1.5K and 100 pF	8kV
ESD Rating Machine Model	400V

10.0 DC and AC Specifications

Note: Typical specifications are at TA=25˚C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

10.1 DC SPECIFICATIONS

TA = -40˚C to +85˚C, V_{CC} = +2.97V to 5.5V, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	3.3V, 10%		5.0V, 10%		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		-0.3	0.6	-0.5	0.6	V
V_{IHX}	Clock Input High Voltage		2.4	5.5	3.1	5.5	V
V_{IL}	Input Low Voltage		-0.3	0.8	-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	5.5	2.2	5.5	V
V_{OL}	Output Low Voltage	I_{OL} = 6mA				0.4	V
		I_{OL} = 4mA		0.4			V
V_{OH}	Output High Voltage	I_{OH} = -6mA			2.4		V
		I_{OH} = -1mA	2.0				V
I_{IL}	Input Low Leakage			10		10	µA
I_{IH}	Input High Leakage			10		10	µA
I_{DD}	Current Consumption	Static clock input		1.6		3.0	mA

10.2 CAPACITANCE

TA = 25˚C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{XIN}	Clock Input Capacitance	f_c = 1 MHz Unmeasured Pins Returned to V_{SS}		7		pF
C_{XOUT}	Clock Output Capacitance			7		pF
C_{IN}	Input Capacitance			5		pF
C_{OUT}	Output Capacitance			6		pF
$C_{I/O}$	Input/Output Capacitance			10		pF

10.3 AC SPECIFICATIONS

TA = -40˚C to +85˚C, V_{CC} = +2.97V to 5.5V, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Condition	3.3V Limits		5.0V Limits		Units
			Min	Max	Min	Max	
f_c	Crystal Frequency			24		24	MHz
t_{HILO}	External Clock Low/High		6		6		ns
f_{OSC}	External Clock Frequency			80		80	MHz
t_{RST}	Reset Pulse Width		70		70		ns
n	Baud Rate Divisor		1	2^{16}-1	1	2^{16}-1	
B_{CLK}	Baud Clock		16 x of data rate				
			1/16 of a bit duration				
Host Interface							
t_{AR}	Address Setup Time		10		10		ns
t_{RA}	Address Hold Time		1		1		ns
t_{RD}	$\overline{RD}$ Strobe Width		35		24		ns
t_{DY}	Read Cycle Delay		35		24		ns
t_{RDV}	Data Access Time			35		24	ns

10.0 DC and AC Specifications (Continued)

Symbol	Parameter	Condition	3.3V Limits		5.0V Limits		Units
			Min	Max	Min	Max	
t_{HZ}	Data Disable Time		0	18	0	18	ns
t_{WR}	$\overline{WR}$ Strobe Width		35		24		ns
t_{DY}	Write Cycle Delay		35		24		ns
t_{DS}	Data Setup Time		12		12		ns
t_{DH}	Data Hold Time		4		4		ns
Modem Control							
t_{MDO}	Delay from $\overline{WR}$ to Output			20		15	ns
t_{SIM}	Delay from Modem input to Interrupt output			20		15	ns
t_{RIM}	Delay to Reset interrupt from $\overline{RD}$ falling edge			23		17	ns
Line Receive and Transmit							
t_{SINT}	Delay from Stop to Interrupt Set	(Note 2)		4		4	Bclk
t_{RINT}	Delay from of $\overline{RD}$ to Reset Interrupt			45		30	ns
t_{STI}	Delay from center of Start to INTR Set			16		10	ns
t_{WST}	Delay from $\overline{WR}$ to Transmit Start		0	16	0	16	Bclk
t_{HR}	Delay from $\overline{WR}$ to interrupt clear			34		22	ns
DMA Interface							
t_{WXI}	Delay from $\overline{WR}$ to $\overline{TXRDY}$ rising edge			27		18	ns
t_{SXA}	Delay from Center of Start to $\overline{TXRDY}$ falling edge			8		8	Bclk
t_{SSR}	Delay from Stop to $\overline{RXRDY}$ falling edge			4		4	Bclk
t_{RXI}	Delay from /RD to $\overline{RXRDY}$ rising edge			27		18	ns

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Note 2: The B_{CLK} period decreases with increasing reference clock input. At higher clock input frequency, the number of B_{CLK} increases.

11.0 Timing Diagrams

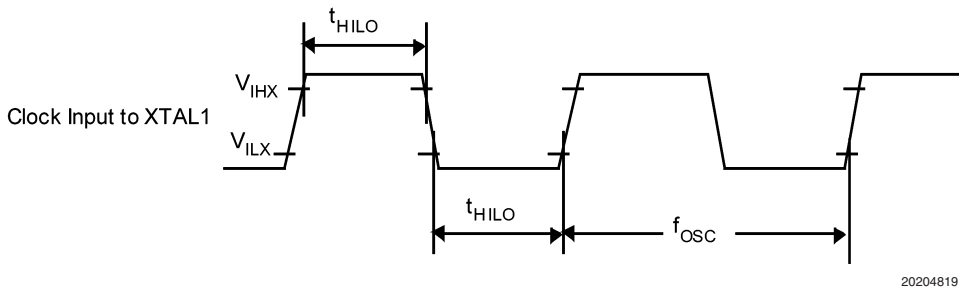


FIGURE 17. External Clock Input

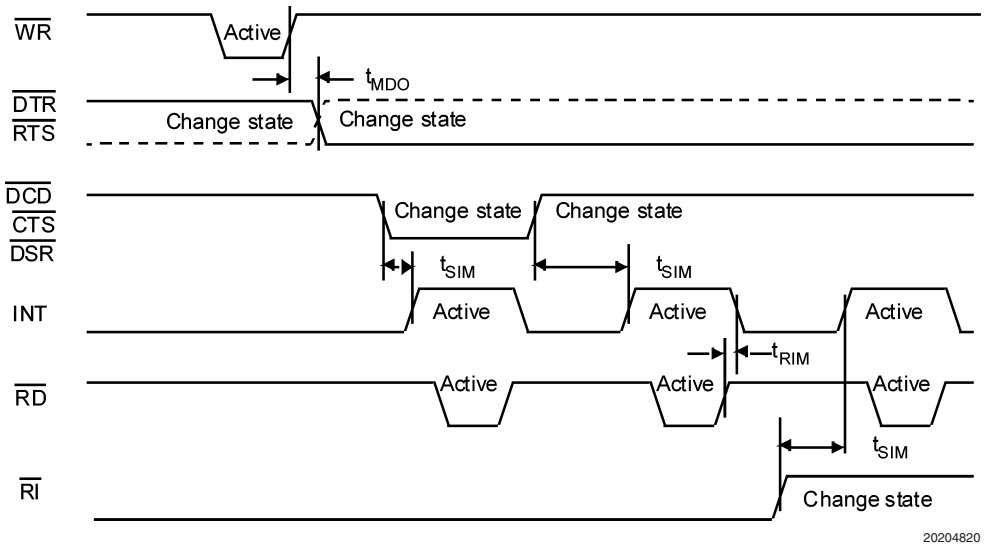


FIGURE 18. Modem Control Timing

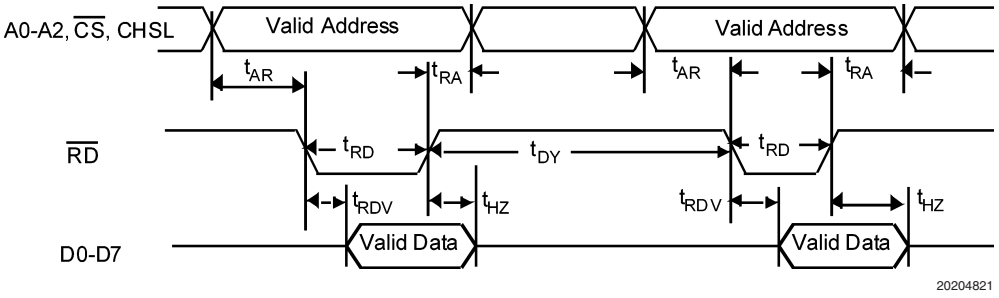


FIGURE 19. Host Interface Read Timing

11.0 Timing Diagrams (Continued)

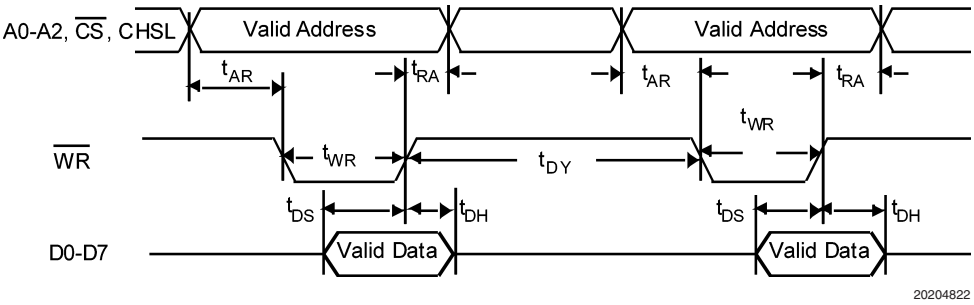


FIGURE 20. Host Interface Write Timing

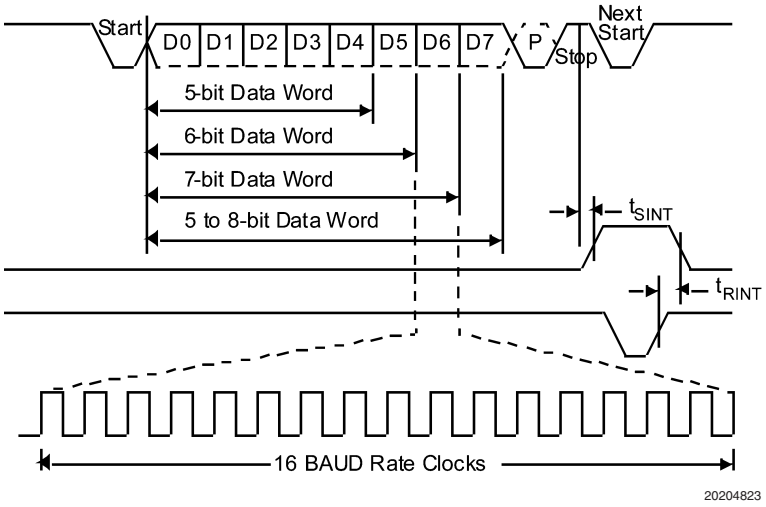


FIGURE 21. Receiver Timing

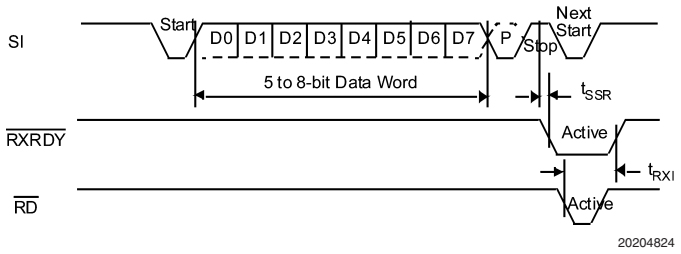


FIGURE 22. Receiver Timing Non-FIFO Mode

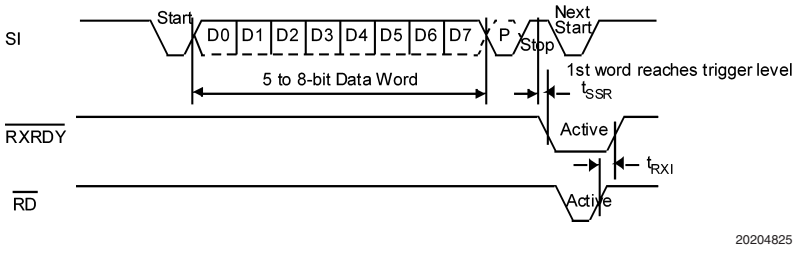


FIGURE 23. Receiver Timing FIFO Mode

11.0 Timing Diagrams (Continued)

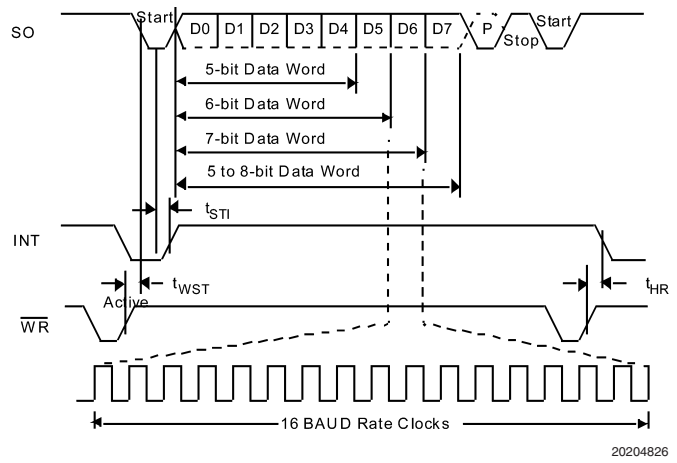


FIGURE 24. Transmitter Timing

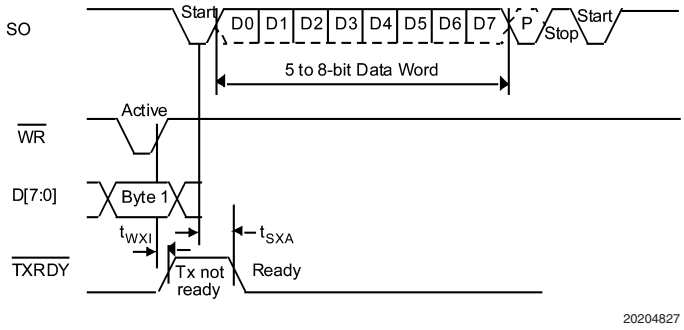


FIGURE 25. Transmitter Timing Non-FIFO Mode

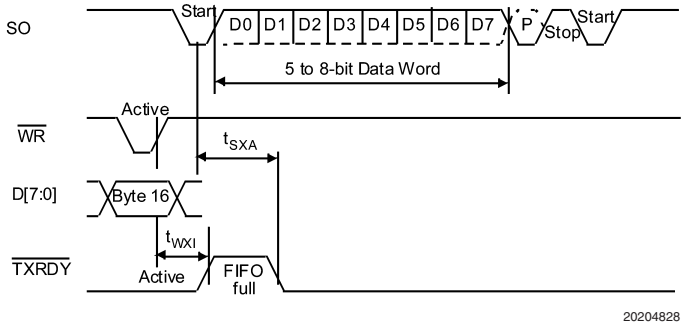
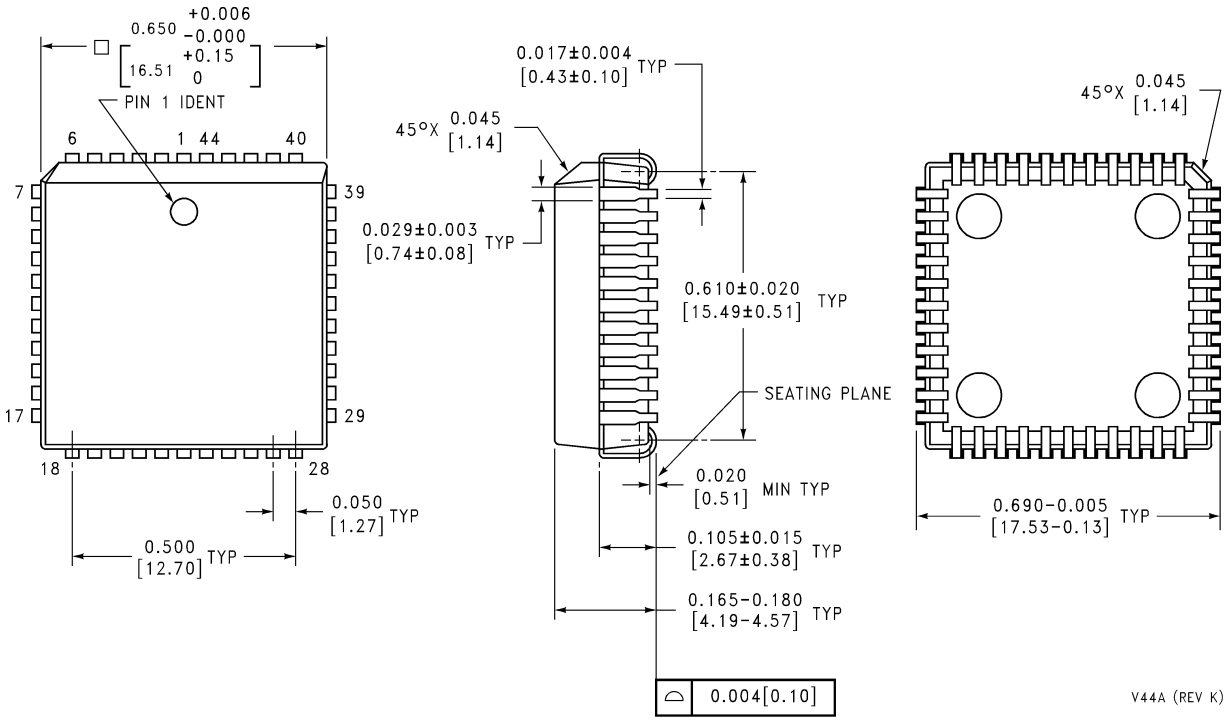
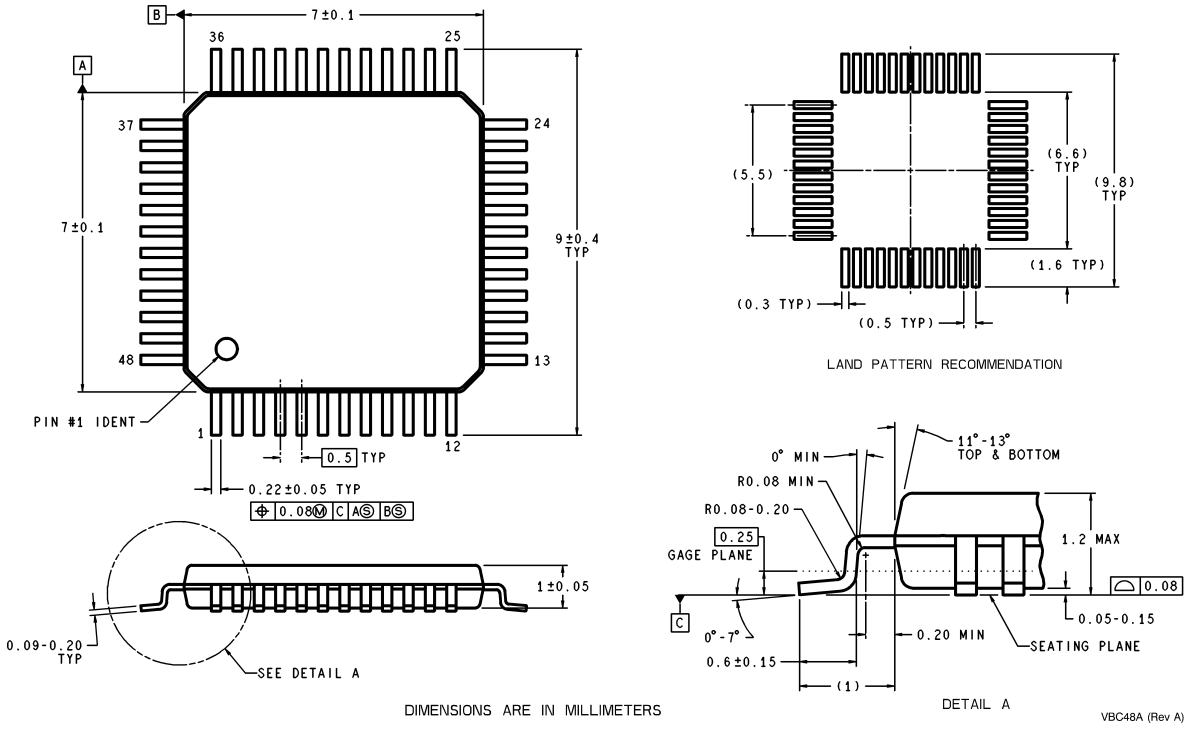


FIGURE 26. Transmitter Timing FIFO Mode

12.0 Physical Dimensions inches (millimeters) unless otherwise noted



44–PLCC Package
Order Number NS16C2552TVA, NS16C2752TVA
NS Package Number V44A



48–TQFP Package
Order Number NS16C2552TVS, NS16C2752TVS
NS Package Number VBC48A

Notes

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