

# LP2950

## Micropower Voltage Regulators

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices feature a very low quiescent bias current of 75  $\mu\text{A}$  and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the Error Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power-on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn-off or turn-on the regulator output.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual-in-line, SO-8 and Micro-8 surface mount packages. The 'A' suffix devices feature an initial output voltage tolerance  $\pm 0.5\%$ .

### LP2950 and LP2951 Features:

- Low Quiescent Bias Current of 75  $\mu\text{A}$
- Low Input-to-Output Voltage Differential of 50 mV at 100  $\mu\text{A}$  and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V  $\pm 0.5\%$  Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0  $\mu\text{F}$  Output Capacitor for Stability
- Internal Current and Thermal Limiting

### LP2951 Additional Features:

- Error Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

(See Following Page for Device Information.)

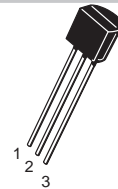


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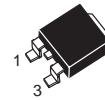
<http://onsemi.com>

**TO-92  
Z SUFFIX  
CASE 29**



Pin: 1. Output  
2. Ground  
3. Input

**DPAK  
DT SUFFIX  
CASE 369A**



### PIN CONNECTIONS

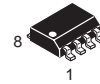


(Top View)

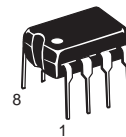
Pin: 1. Input  
2. Ground  
3. Output

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

**SO-8  
D SUFFIX  
CASE 751**



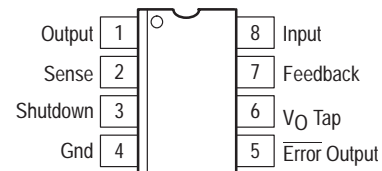
**N SUFFIX  
CASE 626**



**Micro-8  
DM SUFFIX  
CASE 846A**



### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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## DEVICE INFORMATION

Package	Output Voltage				Operating Junction Temperature Range
	3.0V	3.3V	5.0V	Adjustable	
<b>TO-92</b> Suffix Z	LP2950CZ-3.0 LP2950ACZ-3.0	LP2950CZ-3.3 LP2950ACZ-3.3	LP2950CZ-5.0 LP2950ACZ-5.0	Not Available	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$
<b>DKPAK</b> Suffix DT	LP2950CDT-3.0 LP2950ACDT-3.0	LP2950CDT-3.3 LP2950ACDT-3.3	LP2950CDT-5.0 LP2950ACDT-5.0	Not Available	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$
<b>SO-8</b> Suffix D	LP2951CD-3.0 LP2951ACD-3.0	LP2951CD-3.3 LP2951ACD-3.3	LP2951CD LP2951ACD	LP2951CD LP2951ACD	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$
<b>Micro-8</b> Suffix DM	LP2951CDM-3.0 LP2951ACDM-3.0	LP2951CDM-3.3 LP2951ACDM-3.3	LP2951CDM LP2951ACDM	LP2951CDM LP2951ACDM	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$
<b>DIP-8</b> Suffix N	LP2951CN-3.0 LP2951ACN-3.0	LP2951CN-3.3 LP2951ACN-3.3	LP2951CN LP2951ACN	LP2951CN LP2951ACN	$T_J = -40^\circ \text{ to } +125^\circ \text{C}$

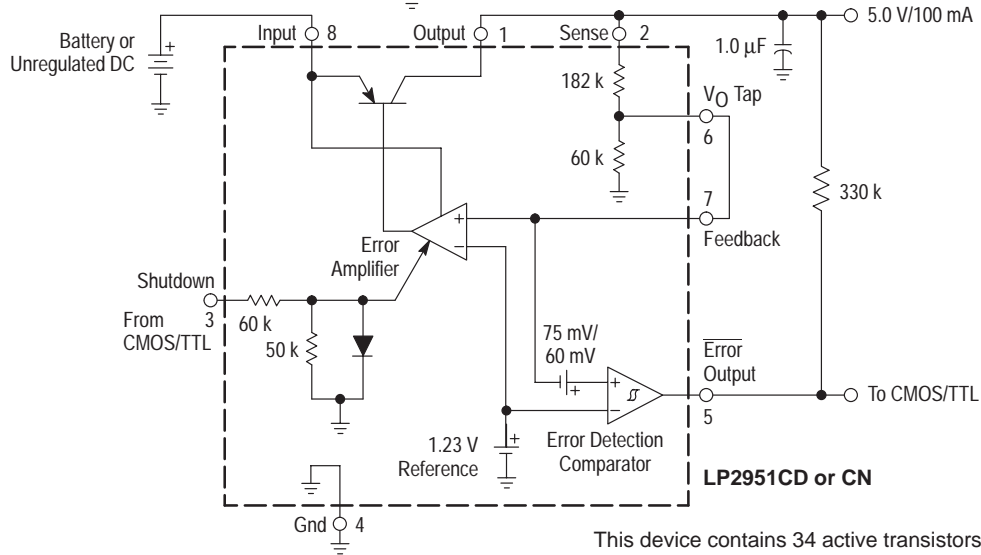
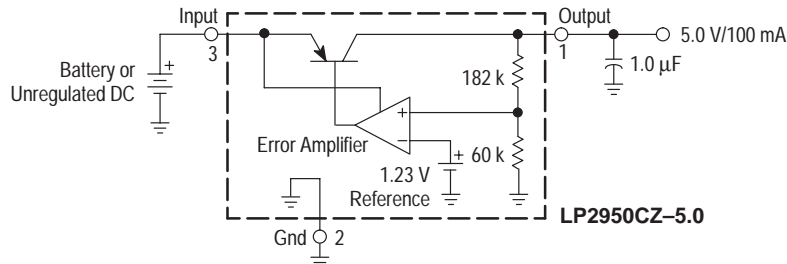
LP2950Cx-xx / LP2951Cxx-xx

1% Output Voltage Precision at  $T_J = 25^\circ \text{C}$

LP2950ACx-xx / LP2951ACxx-xx

0.5% Output Voltage Precision at  $T_J = 25^\circ \text{C}$

### Representative Block Diagrams



This device contains 34 active transistors.

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## MAXIMUM RATINGS (T<sub>A</sub> = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V <sub>CC</sub>	30	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P <sub>D</sub>	Internally Limited	W
Case 751 (SO-8) D Suffix			
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	180	°C/W
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	45	°C/W
Case 369A (DPAK) DT Suffix [Note 1]			
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	92	°C/W
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	6.0	°C/W
Case 29 (TO-226AA/TO-92) Z Suffix			
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	160	°C/W
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	83	°C/W
Case 626 N Suffix			
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	105	°C/W
Case 846A (Micro-8) DM Suffix			
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	240	°C/W
Feedback Input Voltage	V <sub>fb</sub>	-1.5 to +30	Vdc
Shutdown Input Voltage	V <sub>sd</sub>	-0.3 to +30	Vdc
Error Comparator Output Voltage	V <sub>err</sub>	-0.3 to +30	Vdc
Operating Junction Temperature	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

**NOTE:** 1. The Junction-to-Ambient Thermal Resistance is determined by PC board copper area per Figure 26.  
2. ESD data available upon request.

## ELECTRICAL CHARACTERISTICS (V<sub>in</sub> = V<sub>O</sub> + 1.0 V, I<sub>O</sub> = 100 μA, C<sub>O</sub> = 1.0 μF, T<sub>J</sub> = 25°C [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions V <sub>in</sub> = 6.0 V, I <sub>O</sub> = 100 μA, T <sub>J</sub> = 25°C LP2950C-5.0/LP2951C LP2950AC-5.0/LP2951AC T <sub>J</sub> = -40 to +125°C LP2950C-5.0/LP2951C LP2950AC-5.0/LP2951AC V <sub>in</sub> = 6.0 to 30 V, I <sub>O</sub> = 100 μA to 100 mA, T <sub>J</sub> = -40 to +125°C LP2950C-5.0/LP2951C LP2950AC-5.0/LP2951AC	V <sub>O</sub>	4.950 4.975 4.900 4.940 4.880 4.925	5.000 5.000 - - - -	5.050 5.025 5.100 5.060 5.120 5.075	V
Output Voltage, 3.3 V Versions V <sub>in</sub> = 4.3 V, I <sub>O</sub> = 100 μA, T <sub>J</sub> = 25°C LP2950C-3.3/LP2951C-3.3 LP2950AC-3.3/LP2951AC-3.3 T <sub>J</sub> = -40 to +125°C LP2950C-3.3/LP2951C-3.3 LP2950AC-3.3/LP2951AC-3.3 V <sub>in</sub> = 4.3 to 30 V, I <sub>O</sub> = 100 μA to 100 mA, T <sub>J</sub> = -40 to +125°C LP2950C-3.3/LP2951C-3.3 LP2950AC-3.3/LP2951AC-3.3	V <sub>O</sub>	3.267 3.284 3.234 3.260 3.221 3.254	3.300 3.300 - - - -	3.333 3.317 3.366 3.340 3.379 3.346	V
Output Voltage, 3.0 V Versions V <sub>in</sub> = 4.0 V, I <sub>O</sub> = 100 μA, T <sub>J</sub> = 25°C LP2950C-3.0/LP2951C-3.0 LP2950AC-3.0/LP2951AC-3.0 T <sub>J</sub> = -40 to +125°C LP2950C-3.0/LP2951C-3.0 LP2950AC-3.0/LP2951AC-3.0 V <sub>in</sub> = 4.0 to 30 V, I <sub>O</sub> = 100 μA to 100 mA, T <sub>J</sub> = -40 to +125°C LP2950C-3.0/LP2951C-3.0 LP2950AC-3.0/LP2951AC-3.0	V <sub>O</sub>	2.970 2.985 2.940 2.964 2.928 2.958	3.000 3.000 - - - -	3.030 3.015 3.060 3.036 3.072 3.042	V

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**ELECTRICAL CHARACTERISTICS (continued)** ( $V_{in} = V_O + 1.0\text{ V}$ ,  $I_O = 100\ \mu\text{A}$ ,  $C_O = 1.0\ \mu\text{F}$ ,  $T_J = 25^\circ\text{C}$  [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Line Regulation ( $V_{in} = V_{O(nom)} + 1.0\text{ V}$ to $30\text{ V}$ ) [Note 2] LP2950C-XX/LP2951C/LP2951C-XX LP2950AC-XX/LP2951AC/LP2951AC-XX	Reg <sub>line</sub>	– –	0.08 0.04	0.20 0.10	%
Load Regulation ( $I_O = 100\ \mu\text{A}$ to $100\text{ mA}$ ) LP2950C-XX/LP2951C/LP2951C-XX LP2950AC-XX/LP2951AC/LP2951AC-XX	Reg <sub>load</sub>	– –	0.13 0.05	0.20 0.10	%
Dropout Voltage $I_O = 100\ \mu\text{A}$ $I_O = 100\text{ mA}$	$V_I - V_O$	– –	30 350	80 450	mV
Supply Bias Current $I_O = 100\ \mu\text{A}$ $I_O = 100\text{ mA}$	$I_{CC}$	– –	93 4.0	120 12	$\mu\text{A}$ mA
Dropout Supply Bias Current ( $V_{in} = V_{O(nom)} - 0.5\text{ V}$ , $I_O = 100\ \mu\text{A}$ ) [Note 2]	$I_{CC(dropout)}$	–	110	170	$\mu\text{A}$
Current Limit ( $V_O$ Shorted to Ground)	$I_{Limit}$	–	220	300	mA
Thermal Regulation	Reg <sub>thermal</sub>	–	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) [Note 3] $C_L = 1.0\ \mu\text{F}$ $C_L = 100\ \mu\text{F}$	$V_n$	– –	126 56	– –	$\mu\text{V}_{rms}$

## LP2951A/LP2951AC ONLY

Reference Voltage ( $T_J = 25^\circ\text{C}$ ) LP2951C/LP2951C-XX LP2951AC/LP2951AC-XX	$V_{ref}$	1.210 1.220	1.235 1.235	1.260 1.250	V
Reference Voltage ( $T_J = -40$ to $+125^\circ\text{C}$ ) LP2951C/LP2951C-XX LP2951AC/LP2951AC-XX	$V_{ref}$	1.200 1.200	– –	1.270 1.260	V
Reference Voltage ( $T_J = -40$ to $+125^\circ\text{C}$ ) $I_O = 100\ \mu\text{A}$ to $100\text{ mA}$ , $V_{in} = 23$ to $30\text{ V}$ LP2951C/LP2951C-XX LP2951AC/LP2951AC-XX	$V_{ref}$	1.185 1.190	– –	1.285 1.270	V
Feedback Pin Bias Current	$I_{FB}$	–	15	40	nA

## ERROR COMPARATOR

Output Leakage Current ( $V_{OH} = 30\text{ V}$ )	$I_{lkg}$	–	0.01	1.0	$\mu\text{A}$
Output Low Voltage ( $V_{in} = 4.5\text{ V}$ , $I_{OL} = 400\ \mu\text{A}$ )	$V_{OL}$	–	150	250	mV
Upper Threshold Voltage ( $V_{in} = 6.0\text{ V}$ )	$V_{thu}$	40	45	–	mV
Lower Threshold Voltage ( $V_{in} = 6.0\text{ V}$ )	$V_{thl}$	–	60	95	mV
Hysteresis ( $V_{in} = 6.0\text{ V}$ )	$V_{hy}$	–	15	–	mV

## SHUTDOWN INPUT

Input Logic Voltage Logic "0" (Regulator "On") Logic "1" (Regulator "Off")	$V_{shtdn}$	0 2.0	– –	0.7 30	V
Shutdown Pin Input Current $V_{shtdn} = 2.4\text{ V}$ $V_{shtdn} = 30\text{ V}$	$I_{shtdn}$	– –	35 450	50 600	$\mu\text{A}$
Regulator Output Current in Shutdown Mode ( $V_{in} = 30\text{ V}$ , $V_{shtdn} = 2.0\text{ V}$ , $V_O = 0$ , Pin 6 Connected to Pin 7)	$I_{off}$	–	3.0	10	$\mu\text{A}$

- NOTES:**  
 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 2.  $V_{O(nom)}$  is the part number voltage option.  
 3. Noise tests on the LP2951 are made with a  $0.01\ \mu\text{F}$  capacitor connected across Pins 7 and 1.

DEFINITIONS

**Dropout Voltage** – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

**Line Regulation** – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

**Load Regulation** – The change in output voltage for a change in load current at constant chip temperature.

**Maximum Power Dissipation** – The maximum total device dissipation for which the regulator will operate within specifications.

**Bias Current** – Current which is used to operate the regulator chip and is not delivered to the load.

**Output Noise Voltage** – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Leakage Current** – Current drawn through a bipolar transistor collector–base junction, under a specified collector voltage, when the transistor is “off”.

**Upper Threshold Voltage** – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “0” to “1”.

**Lower Threshold Voltage** – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic “1” to “0”.

**Hysteresis** – The difference between Lower Threshold voltage and Upper Threshold voltage.

Figure 1. Quiescent Current

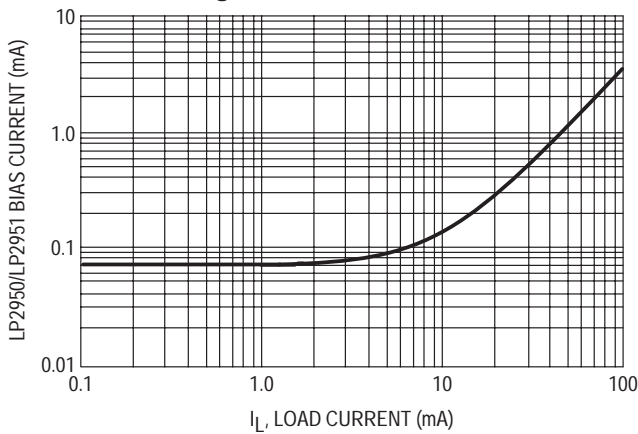


Figure 2. Dropout Characteristics

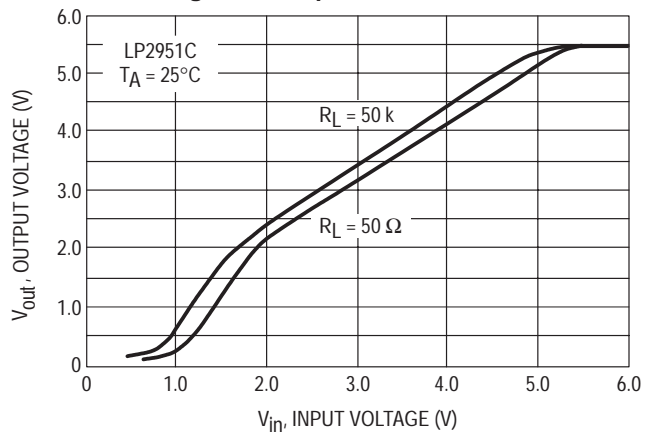


Figure 3. Input Current

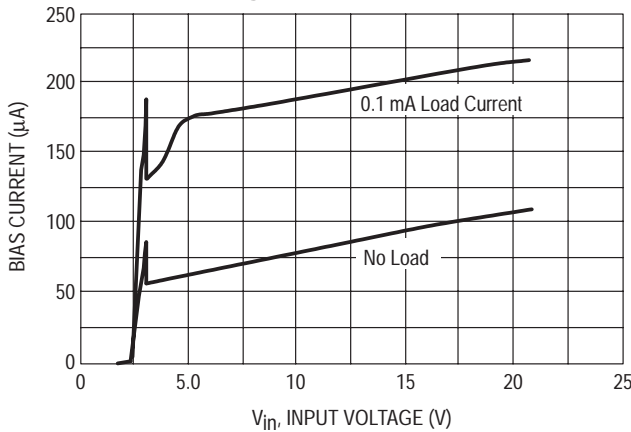
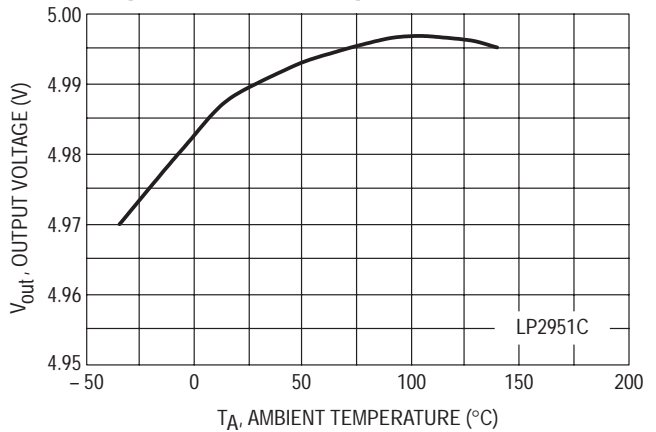
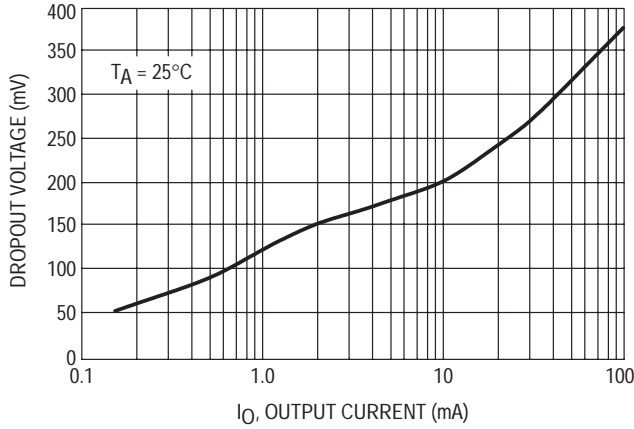


Figure 4. Output Voltage versus Temperature

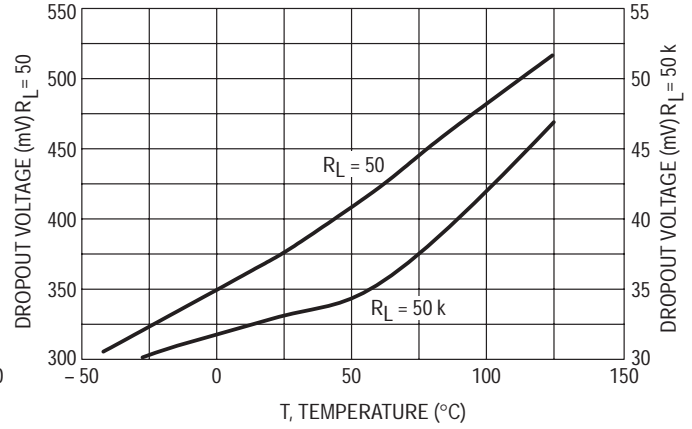


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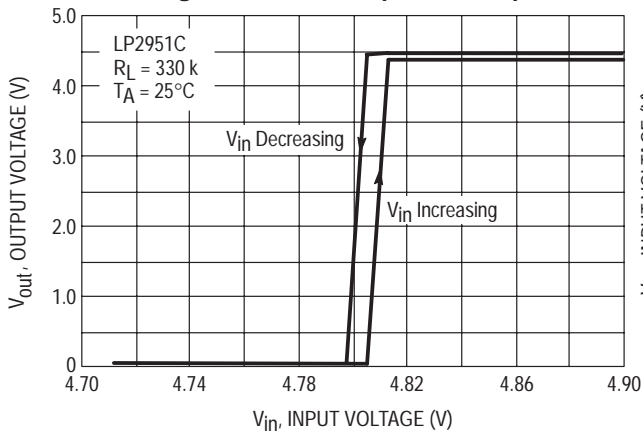
**Figure 5. Dropout Voltage versus Output Current**



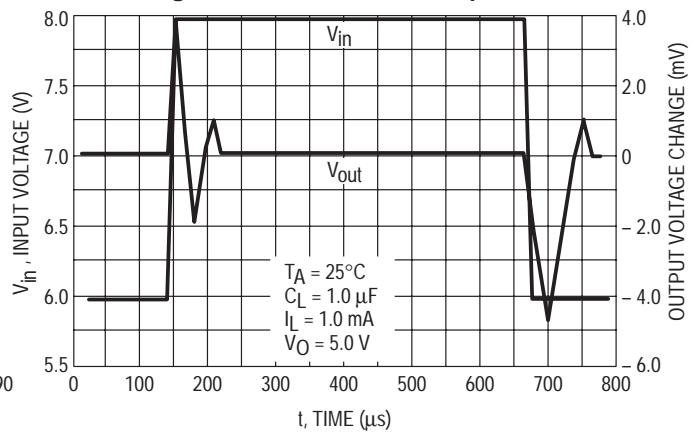
**Figure 6. Dropout Voltage versus Temperature**



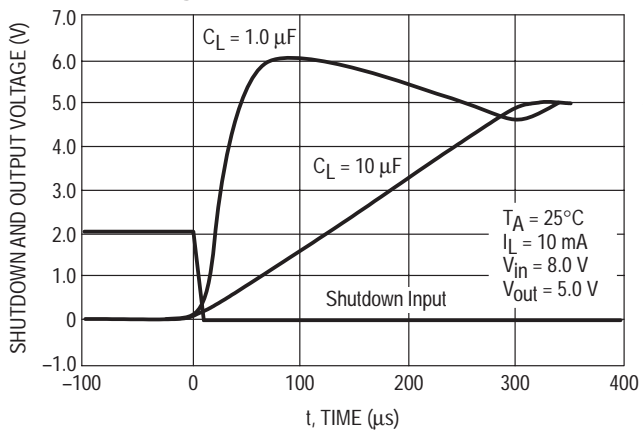
**Figure 7. Error Comparator Output**



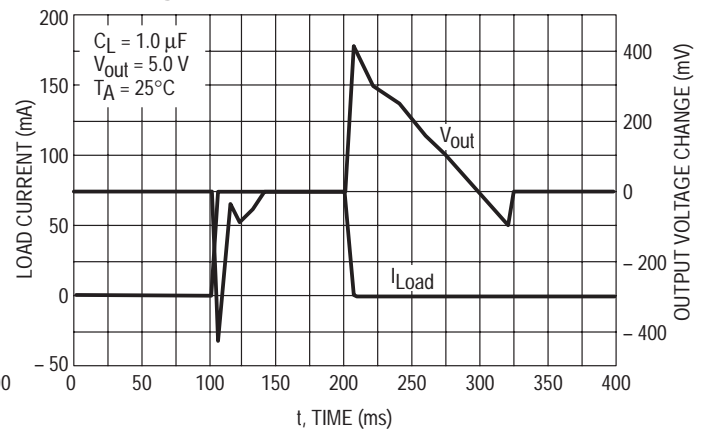
**Figure 8. Line Transient Response**



**Figure 9. LP2951 Enable Transient**

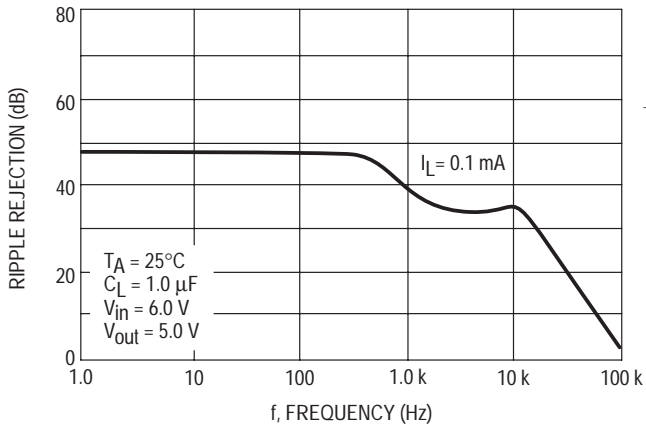


**Figure 10. Load Transient Response**

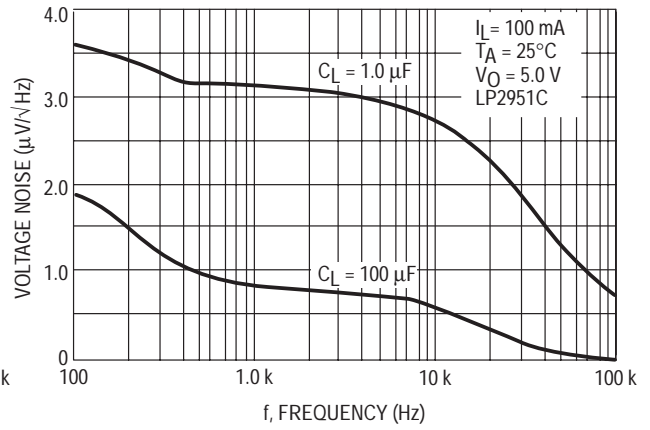


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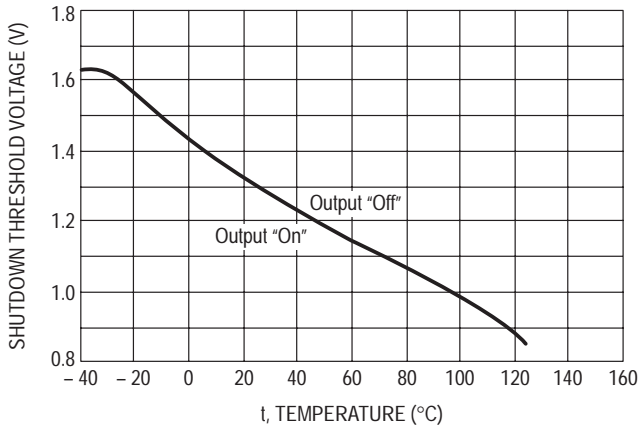
**Figure 11. Ripple Rejection**



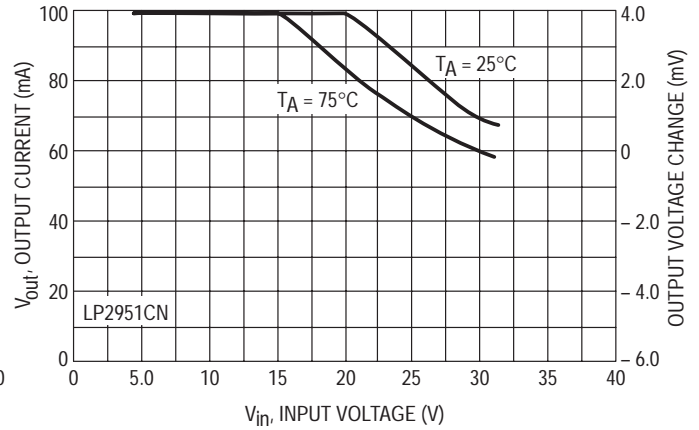
**Figure 12. Output Noise**



**Figure 13. Shutdown Threshold Voltage versus Temperature**



**Figure 14. Maximum Rated Output Current**



APPLICATIONS INFORMATION

Introduction

The LP2950/LP2951 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Typical application circuits for the LP2950 and LP2951 are shown in Figures 17 through 25.

These regulators are not internally compensated and thus require a 1.0  $\mu\text{F}$  (or greater) capacitance between the LP2950/LP2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33  $\mu\text{F}$  for currents less than 10 mA, or 0.1  $\mu\text{F}$  for currents below 1.0 mA. Using the 8-pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (Output Pin 1 connected to the feedback Pin 7) a minimum capacitance of 3.3  $\mu\text{F}$  is recommended.

The LP2950 will remain stable and in regulation when operated with no output load. When setting the output voltage of the LP2951 with external resistors, the resistance values should be chosen to draw a minimum of 1.0  $\mu\text{A}$ .

A bypass capacitor is recommended across the LP2950/LP2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor.

Input capacitance at the LP2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least 3.3  $\mu\text{F}$  will stabilize the feedback loop.

Error Detection Comparator

The comparator switches to a positive logic low whenever the LP2951 output voltage falls more than approximately 5.0% out of regulation. This value is the comparator's designed-in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains 5.0% below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

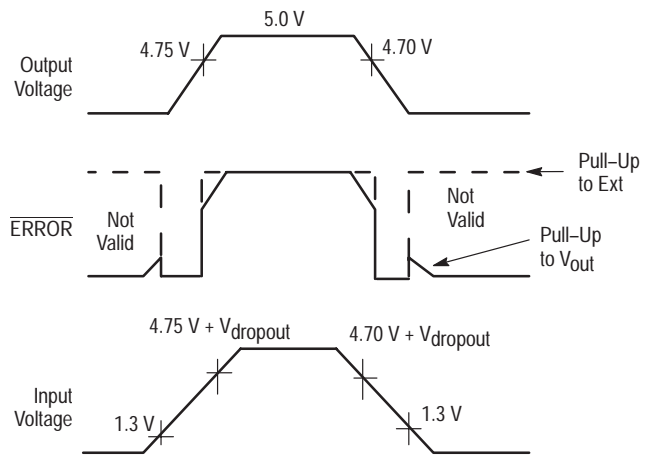
Figure 1 is a timing diagram which shows the  $\overline{\text{ERROR}}$  signal and the regulated output voltage as the input voltage

to the LP2951 is ramped up and down. The  $\overline{\text{ERROR}}$  signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V ( $V_{\text{out}}$  exceeds about 4.75 V). Since the LP2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.

The error comparator output is an open collector which requires an external pull-up resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the 400  $\mu\text{A}$  sink capability of the error comparator. A value between 100 k and 1.0 M $\Omega$  is suggested. No pull-up resistance is required if this output is unused.

When operated in the shutdown mode, the error comparator output will go high if it has been pulled up to an external supply. To avoid this invalid response, the error comparator output should be pulled up to  $V_{\text{out}}$  (see Figure 15).

Figure 15. ERROR Output Timing

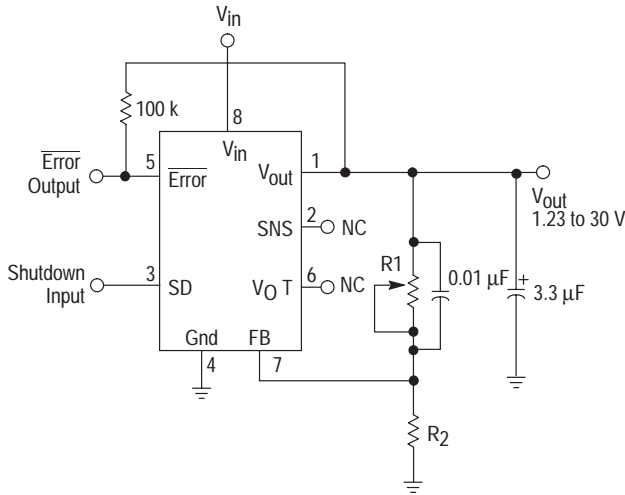


Programming the Output Voltage (LP2951)

The LP2951CX may be pin-strapped for 5.0 V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 16.



Figure 16. Adjustable Regulator



The complete equation for the output voltage is:

$$V_{out} = V_{ref} (1 + R1/R2) + I_{FB} R1$$

where  $V_{ref}$  is the nominal 1.235 V reference voltage and  $I_{FB}$  is the feedback pin bias current, nominally  $-20$  nA. The minimum recommended load current of  $1.0$   $\mu$ A forces an upper limit of  $1.2$  M $\Omega$  on the value of  $R2$ , if the regulator must work with no load.  $I_{FB}$  will produce a 2% typical error in  $V_{out}$  which may be eliminated at room temperature by adjusting  $R1$ . For better accuracy, choosing  $R2 = 100$  k reduces this error to 0.17% while increasing the resistor program current to  $12$   $\mu$ A. Since the LP2951 typically draws  $75$   $\mu$ A at no load with Pin 2 open circuited, the extra  $12$   $\mu$ A of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

### Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise on the 3 lead LP2950. However, increasing the capacitor from  $1.0$   $\mu$ F to  $220$   $\mu$ F only

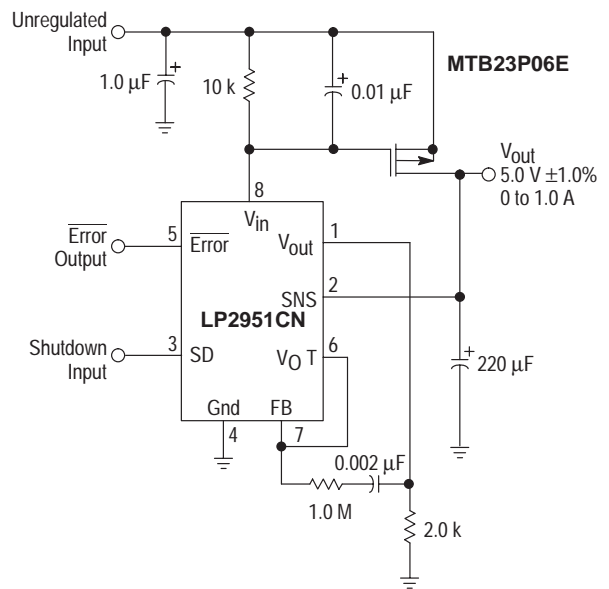
decreases the noise from  $430$   $\mu$ V to  $160$   $\mu$ Vrms for a  $100$  kHz bandwidth at the  $5.0$  V output.

Noise can be reduced fourfold by a bypass capacitor across  $R1$ , since it reduces the high frequency gain from 4 to unity. Pick

$$C_{Bypass} \approx \frac{1}{2\pi R1 \times 200 \text{ Hz}}$$

or about  $0.01$   $\mu$ F. When doing this, the output capacitor must be increased to  $3.3$   $\mu$ F to maintain stability. These changes reduce the output noise from  $430$   $\mu$ V to  $126$   $\mu$ Vrms for a  $100$  kHz bandwidth at  $5.0$  V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Figure 17. 1.0 A Regulator with 1.2 V Dropout



# LP2950

## TYPICAL APPLICATIONS

Figure 18. Lithium Ion Battery Cell Charger

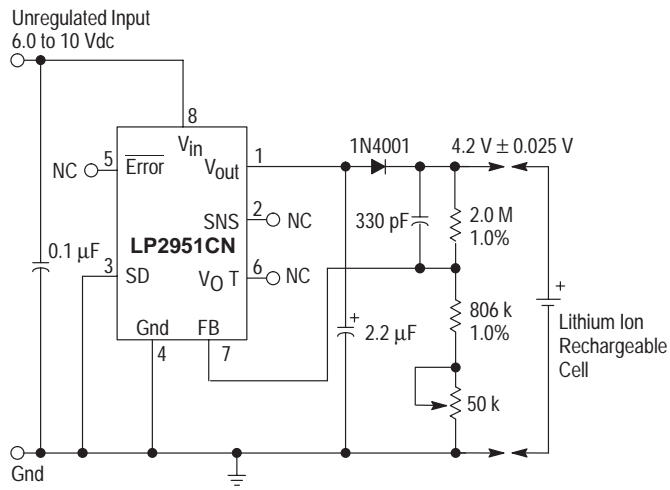


Figure 19. Low Drift Current Sink

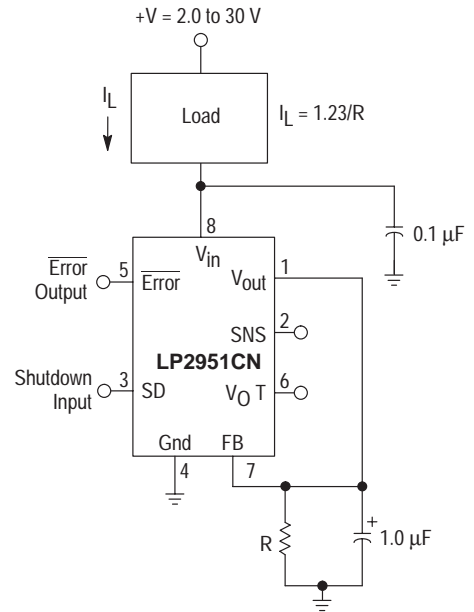
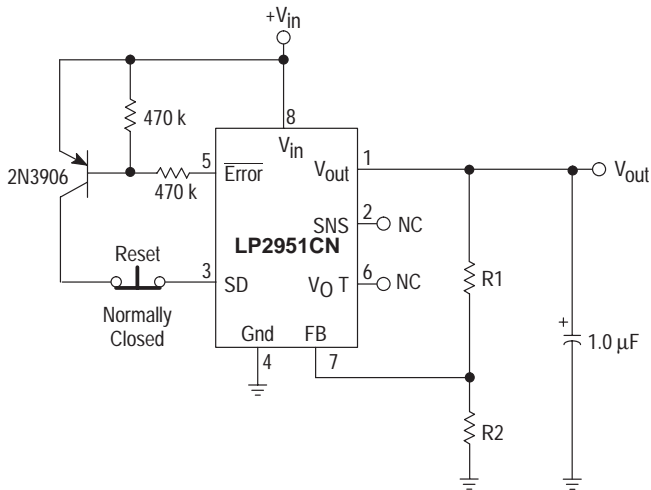
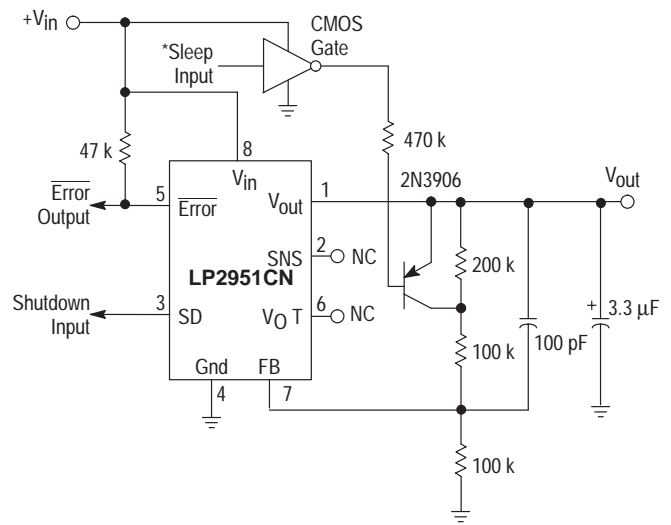


Figure 20. Latch Off When Error Flag Occurs



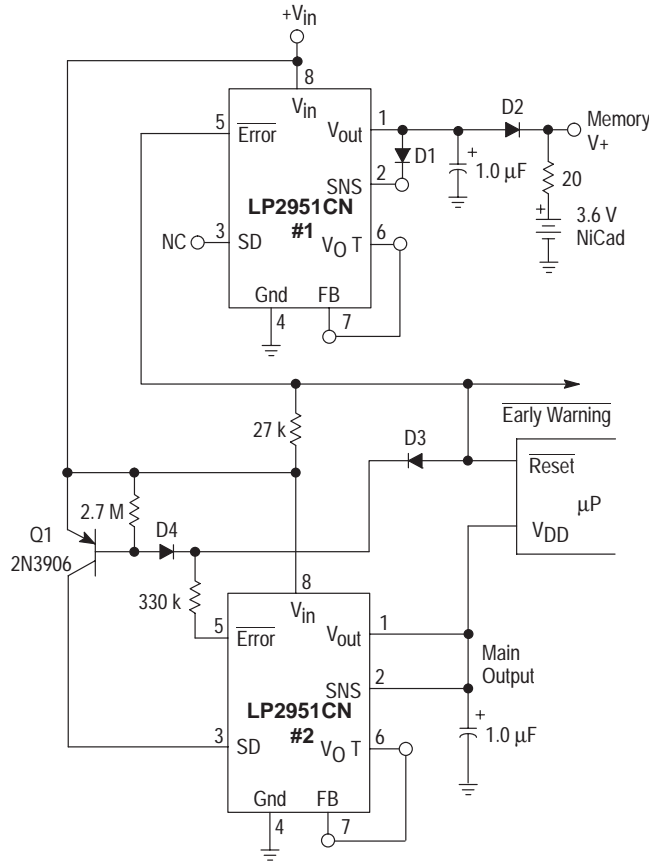
Error flag occurs when  $V_{in}$  is too low to maintain  $V_{out}$ , or if  $V_{out}$  is reduced by excessive load current.

Figure 21. 5.0 V Regulator with 2.5 V Sleep Function



# LP2950

**Figure 22. Regulator with Early Warning and Auxiliary Output**



All diodes are 1N4148.

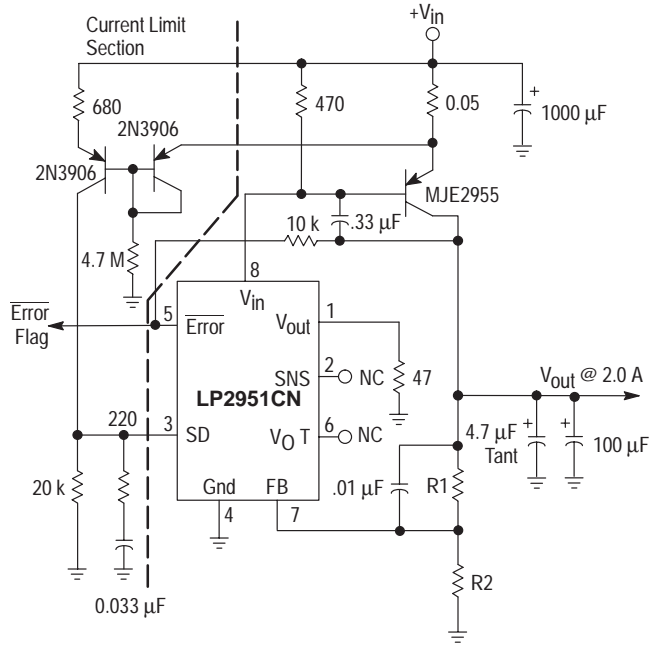
Early Warning flag on low input voltage.

Main output latches off at lower input voltages.

Battery backup on auxiliary output.

Operation: Regulator #1's  $V_{out}$  is programmed one diode drop above 5.0 V. Its error flag becomes active when  $V_{in} \leq 5.7$  V. When  $V_{in}$  drops below 5.3 V, the error flag of regulator #2 becomes active and via Q1 latches the main output "off". When  $V_{in}$  again exceeds 5.7 V, regulator #1 is back in regulation and the early warning signal rises, unlatching regulator #2 via D3.

**Figure 23. 2.0 A Low Dropout Regulator**



$$V_{out} = 1.25V (1.0 + R1/R2)$$

For 5.0 V output, use internal resistors. Wire Pin 6 to 7, and wire Pin 2 to  $+V_{out}$  Bus.

# LP2950

Figure 24. Open Circuit Detector for 4.0 to 20 mA Current Loop

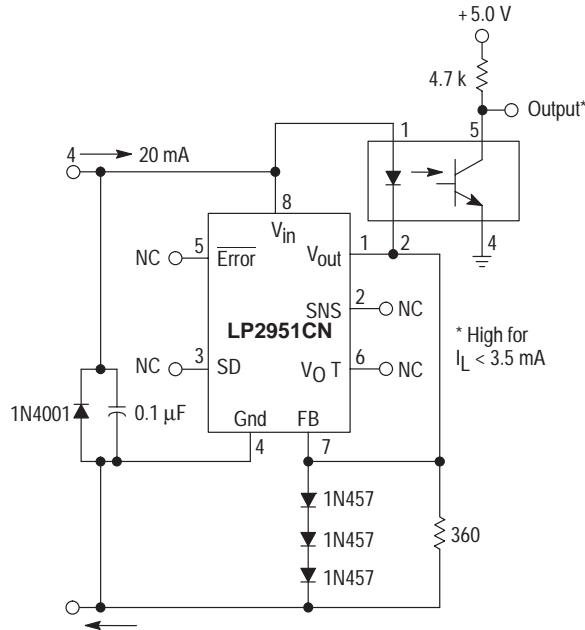


Figure 25. Low Battery Disconnect

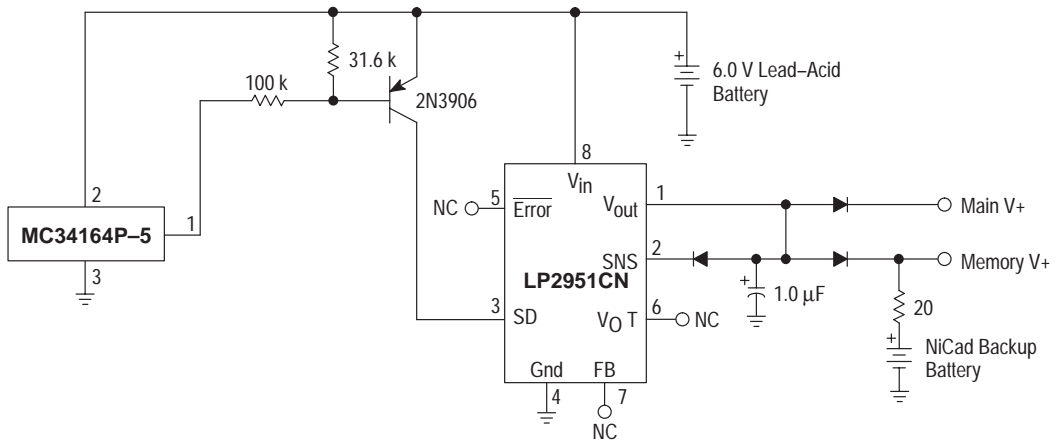
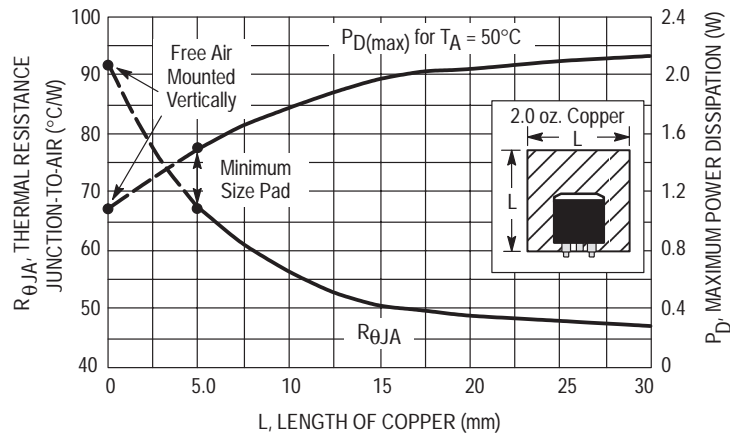


Figure 26. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



# LP2950

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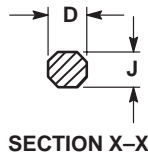
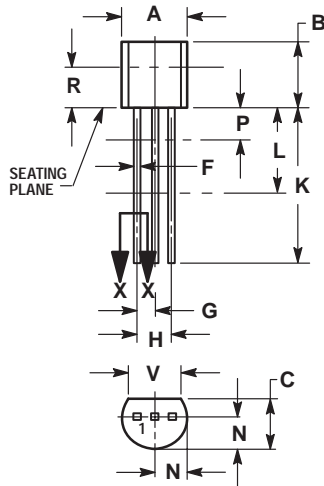
Part Number	Package	Shipping
LP2950CZ-3.0RA	TO-92	2000 units / Tape & Reel
LP2950ACZ-3.0RA	TO-92	2000 units / Tape & Reel
LP2950CZ-3.3RA	TO-92	2000 units / Tape & Reel
LP2950ACZ-3.3RA	TO-92	2000 units / Tape & Reel
LP2950CZ-5.0RA	TO-92	2000 units / Tape & Reel
LP2950ACZ-5.0RA	TO-92	2000 units / Tape & Reel
LP2950CDT-3.0	DPAK	75 units / Rail
LP2950CDT-3.0RK	DPAK	2500 units / Tape & Reel
LP2950ACDT-3.0	DPAK	75 units / Rail
LP2950ACDT-3.0RK	DPAK	2500 units / Tape & Reel
LP2950CDT-3.3	DPAK	75 units / Rail
LP2950CDT-3.3RK	DPAK	2500 units / Tape & Reel
LP2950ACDT-3.3	DPAK	75 units / Rail
LP2950ACDT-3.3RK	DPAK	2500 units / Tape & Reel
LP2950CDT-5.0	DPAK	75 units / Rail
LP2950CDT-5.0RK	DPAK	2500 units / Tape & Reel
LP2950ACDT-5.0	DPAK	75 units / Rail
LP2950ACDT-5.0RK	DPAK	2500 units / Tape & Reel

LP2951CD-3.0	SO-8	98 units / Rail
LP2951CD-3.0R2	SO-8	2500 units / Tape & Reel
LP2951ACD-3.0	SO-8	98 units / Rail
LP2951ACD-3.0R2	SO-8	2500 units / Tape & Reel
LP2951CD-3.3	SO-8	98 units / Rail
LP2951CD-3.3R2	SO-8	2500 units / Tape & Reel
LP2951ACD-3.3	SO-8	98 units / Rail
LP2951ACD-3.3R2	SO-8	2500 units / Tape & Reel
LP2951CD	SO-8	98 units / Rail
LP2951CDR2	SO-8	2500 units / Tape & Reel
LP2951ACD	SO-8	98 units / Rail
LP2951ACDR2	SO-8	2500 units / Tape & Reel
LP2951CDM-3.0R2	Micro-8	2500 units / Tape & Reel
LP2951ACDM-3.0R2	Micro-8	2500 units / Tape & Reel
LP2951CDM-3.3R2	Micro-8	2500 units / Tape & Reel
LP2951ACDM-3.3R2	Micro-8	2500 units / Tape & Reel
LP2951CDMR2	Micro-8	2500 units / Tape & Reel
LP2951ACDMR2	Micro-8	2500 units / Tape & Reel
LP2951CN-3.0	DIP-8	50 units / Rail
LP2951ACN-3.0	DIP-8	50 units / Rail
LP2951CN-3.3	DIP-8	50 units / Rail
LP2951ACN-3.3	DIP-8	50 units / Rail
LP2951CN	DIP-8	50 units / Rail
LP2951ACN	DIP-8	50 units / Rail

# LP2950

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 CASE 29-04  
 ISSUE AD

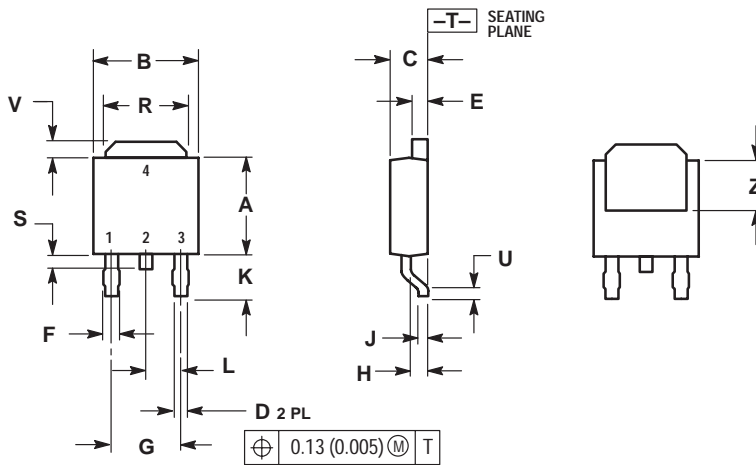


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1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

**DT SUFFIX**  
**(DPAK)**  
 PLASTIC PACKAGE  
 CASE 369A-13  
 ISSUE Y



**NOTES:**

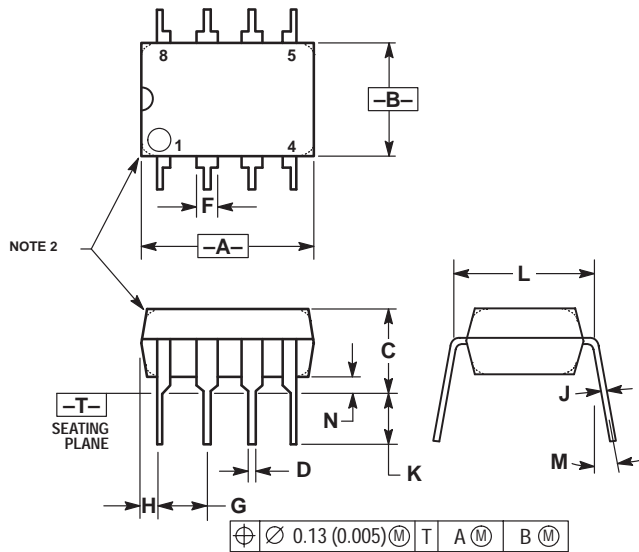
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC	---	4.58 BSC	---
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC	---	2.29 BSC	---
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

# LP2950

## PACKAGE DIMENSIONS

**N SUFFIX**  
 PLASTIC PACKAGE  
 CASE 626-05  
 ISSUE K

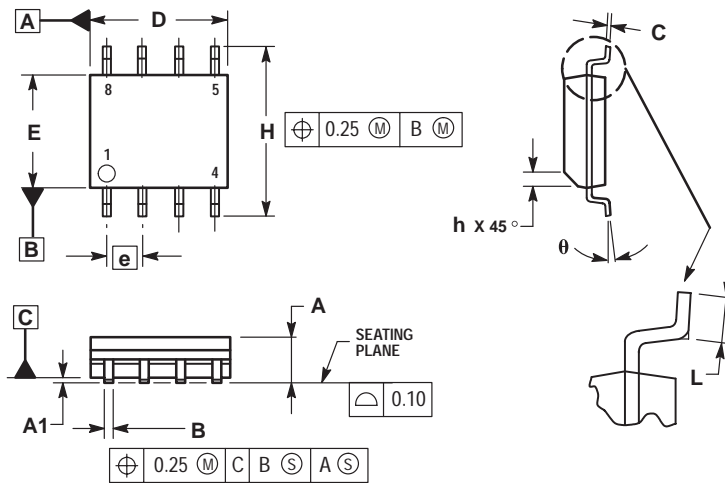


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	-	10°	-	10°
N	0.76	1.01	0.030	0.040

**D SUFFIX**  
**(SO-8)**  
 PLASTIC PACKAGE  
 CASE 751-05  
 ISSUE R



NOTES:

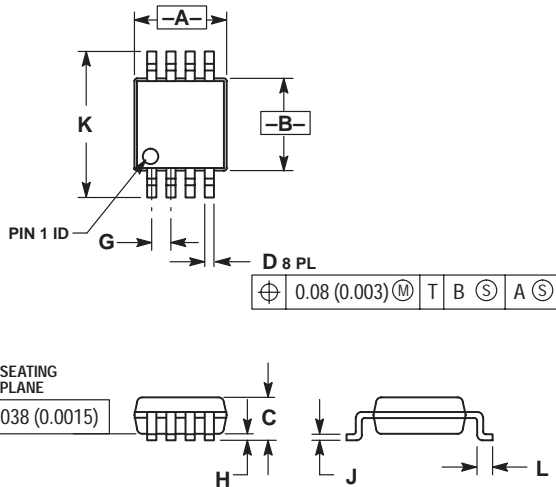
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

# LP2950

## PACKAGE DIMENSIONS


DM SUFFIX  
(Micro-8)  
PLASTIC PACKAGE  
CASE 846A-02  
ISSUE C



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

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